

TABLE I. DEVICE PARAMETERS 1/

JPL PART #	PART NO. TO BE MARKED ON PART	MFR.	GENERIC PART NO.	RADIATION LEVEL (TID) (RAD) 2/	PACKAGE STYLE	TERMINAL CONNECTIONS	ELECTRICAL PERFORMANCE CHARACTERISTICS	ELECTRICAL TEST REQUIREMENTS	BURN-IN CIRCUITS
ST12187	12187-UT25ERISB	UTMC	UT25ER	100K	FIGURE 6.3 HEREIN (196-LEAD FLAT PACK)	TABLE 2-1 HEREIN	TABLES 5-4, 5-5 HEREIN	TABLE 5-1 HEREIN	TABLE 5-6 HEREIN

- NOTES: 1/ THIS DRAWING, IN CONJUNCTION WITH CS515577, REV. C, IMPOSES ALL REQUIREMENTS FOR PROCUREMENT OF THESE DEVICES, WITH THE FOLLOWING EXCEPTIONS:
- A. STATISTICAL PROCESS CONTROL TECHNIQUES SHALL BE SUBSTITUTED FOR 100% NON-DESTRUCTIVE BOND PULL.
 - B. TRACEABILITY SHALL BE MAINTAINED TO THE INDIVIDUAL WAFER.
 - C. ORGANIC OR POLYMERIZED MATERIAL MAY BE USED INSIDE THE PACKAGE IF APPROVED BY JPL.
 - D. IDDQ TESTING SHALL BE PERFORMED.
- 2/ TOTAL DOSE REQUIREMENTS: THE MANUFACTURER SHALL PERFORM TOTAL DOSE TESTING PER MIL-STD-883 METHOD 5005 GROUP E AND METHOD 1019.4. SAMPLES SHALL MEET THE PERFORMANCE CHARACTERISTICS OF TABLE I AT AN AMBIENT TEMPERATURE OF 25 DEGREES C AFTER AN ACCUMULATED DOSE OF 100 KRAD(Si).
- 3/ THIS STANDARD TAKES PRECEDENCE OVER DOCUMENTS REFERENCED HEREIN.

RELEASED THROUGH SECTION 356 DATA MANAGEMENT			DATE:
REVISION: B		APPROVED BY: Dean A. Miller (Sec. 344)	DATE:
		APPROVED BY: Frank R. Stott (Sec. 507)	DATE:
APPROVED SOURCE(S)			
VENDOR PART NO.	VENDOR	JPL PART NO.	ONLY THE ITEM LISTED IN THE APPROVED SOURCE BLOCK AND IDENTIFIED BY VENDOR NAME, ADDRESS, AND PART NUMBER HAS BEEN EVALUATED AND APPROVED BY THE JET PROPULSION LABORATORY OR ITS DELEGATED ALTERNATE. A SUBSTITUTE ITEM SHALL NOT BE USED WITHOUT PRIOR EVALUATION AND APPROVAL BY JPL OR ITS DELEGATED ALTERNATE.
See Table I	UNITED TECHNOLOGIES MICROELECTRONICS CENTER (UTMC) 1575 GARDEN OF THE GODS ROAD COLORADO SPRINGS, COLORADO 80907-3486 CAGE NO. 65342	12187-UT25ERISB	
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Procurement specification: CS515577	TITLE: MICROCIRCUIT, MONOLITHIC CMOS, GATE ARRAY, INTER-SUBASSEMBLY BUS ASIC	JPL CAGE NO: 23835	
Screening specification: ZPP-2073-GEN		ST12187	
Custodian: Electronic Parts Engineering Section 507		SHEET 1 OF 47	

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Scope

This document is a procurement specification for the Inter-Subassembly Bus Gate Array (ISBGA) application specific integrated circuit (ASIC). It represents the functional specifications for the ISBGA along with its electrical characteristics, physical characteristics and device level statistics.

This document shall be the sole source of design and procurement specifications for the ISBGA, and shall supersede any other specification documents issued prior to this release.

Applicable Documents

- General Specifications for Microcircuits, CS515577, Rev. C, 13 May 1991.
This document establishes the general design system, manufacturing and testing requirements for the gate array Application Specific Integrated Circuit (ASIC) parts.
- Any applicable exceptions to CS515577, Rev. C, as defined in section 8 of this drawing.
- MIL-I-38535, Integrated Circuits (Microcircuits) Manufacturing, General Specification for
- MIL-STD-883, Test Methods and Procedures for Microelectronics
- JPL Specification ES516362, Rev. E, Inter-Subassembly Bus Gate Array Design Specification

Primary sources of functional and environmental requirements for this device:

- JPL Drawing 10142395, EFC ISB Interface Circuit Data Sheet
- JPL Document CAS-4-2007, Cassini Orbiter Functional Requirements, AACS, and ECR 80132, AACS Fault Protection
- JPL Specification ES515831, Engineering Flight Computer Specification
- JPL Specification ES516347, Attitude and Articulation Control Flight Computer Specification
- JPL Document AACS-ICD516361, Cassini AACS Interface Control Document

Conventions Used

ISBGA signals are active low (low true logic) if they are designated with "_B" after a signal name. All other signals are active high (high true logic). In the functional description section, an "*" after a signal name may be used to designate active low signals external to the ISBGA.

Signal names prefixed with an L (for local) denote buffered versions of ISB signals as defined in JPL Drawing 10142395. Signal names prefixed with a C denote client interface signals, and signal names prefixed with a P denote pixel interface signals.

Signal names ending in I denote buffered unidirectional input versions of ISB signals as defined in JPL Drawing 10142395. Signal names ending in O denote buffered unidirectional output versions of ISB signals as defined in JPL Drawing 10142395.

In the register descriptions, HBit refers to the hardware bit number scheme in which HBit 0 is the least significant bit (LSB). SBit refers to the EFC software nomenclature in which SBit 0 is the most significant bit (MSB).

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Additional Requirements

a. Functional delay simulation: To be derived from each final application specific electrical design and layout (i.e. post-routing design). Simulation shall be accomplished by using actual delays as computed from the placement and layout of the device as it will be fabricated. Actual delays shall include the contribution associated with the delay through the gate as well as the contribution due to actual metal capacitance and loading on the output(s). Using these actual delays, the application specific design shall insure the absence of timing violations in the circuit. Such timing violations shall include, but shall not be limited to, setup, hold, critical delay path, and circuit race conditions due to variations in process, temperature, supply voltage and radiation. The simulated circuit behavior at the two (fast and slow) worst case extremes of temperature, supply voltage and process shall be identical states at the specified strobe time (usually at the end of a typical strobe cycle where all signals are stable).

Note: All timing parameters indicated in Manufacturer's data books shall be checked in timing simulation.

b. Layout verification: Mask level design rule checks, electrical rule checks, and connectivity checks for each application specific design shall be accomplished. The manufacturer will explain any rules not checked and all error reports produced by the checker. Rule checking will encompass the following rules set:

b1. Design layout rules as a manufacturer's controlled document.

b2. A list of the macros in the manufacturer's macro cell library, macro cell performance data, and macro cell simulation verification data. Performance data shall be guaranteed for all hard macrocells. Soft macrocells in the Manufacturer's library will perform to specifications regardless of layout. For the Manchester Decoder macro, the applicable specification is MIL-STD-1553B.

b3. Process control monitor design used by the manufacturer for qualification and wafer acceptance.

b4. Software packages internally developed (and not acquired from outside sources) and used by the manufacturer in the gate array design process.

b5. Design rule check (DRC) and electrical rule check (ERC) software verification. The manufacturer's DRC and ERC software shall be run on a design that contains known rule violations; the output shall be presented and must show that violations were flagged.

b6. Layout versus schematic (LVS) checker. Manufacturer must demonstrate the effectiveness of the LVS software. The LVS check will ensure that the layout matches exactly the logic schematic simulated by the application specific integrated circuit (ASIC) designer.

b7. Fault simulator used for fault grading is Verifault.

c. Power routing analysis: Derived from each application specific electrical design and layout. The worst case analysis of power buses shall show that at no time shall the localized bus current density exceed specification for bus current density of power bus material as defined in CS 515577 (rev. C). Power routing analysis must be based upon the actual placement of cells within the array. A worst case analysis may be performed instead of the analysis based on actual cell placement; the worst case analysis must be approved by JPL.

d. Test vectors: The test vectors shall be supplied on a magnetic tape and shall be identified by test tape number and revision letter.

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1. CHIP OVERVIEW

The Inter-Subassembly Bus Gate Array implements the following functions:

- Provides the bus interface logic between the ISB and the SUROM, BCIU, PIU and BAU.
- Provides arbitration logic to arbitrate between BCIU and ISB.
- Contains a 16-bit EDAC (error correction and detection unit) based on the commercial 39C60.
- Provides an interface to allow slave access to client devices through the ISB.
- Provides an interface to allow slave access to status registers.
- Provides an interface to allow master access by the PIU to the ISB.
- Provides control logic for pixel collection.
- Provides arbitration logic to arbitrate master accesses on the ISB.

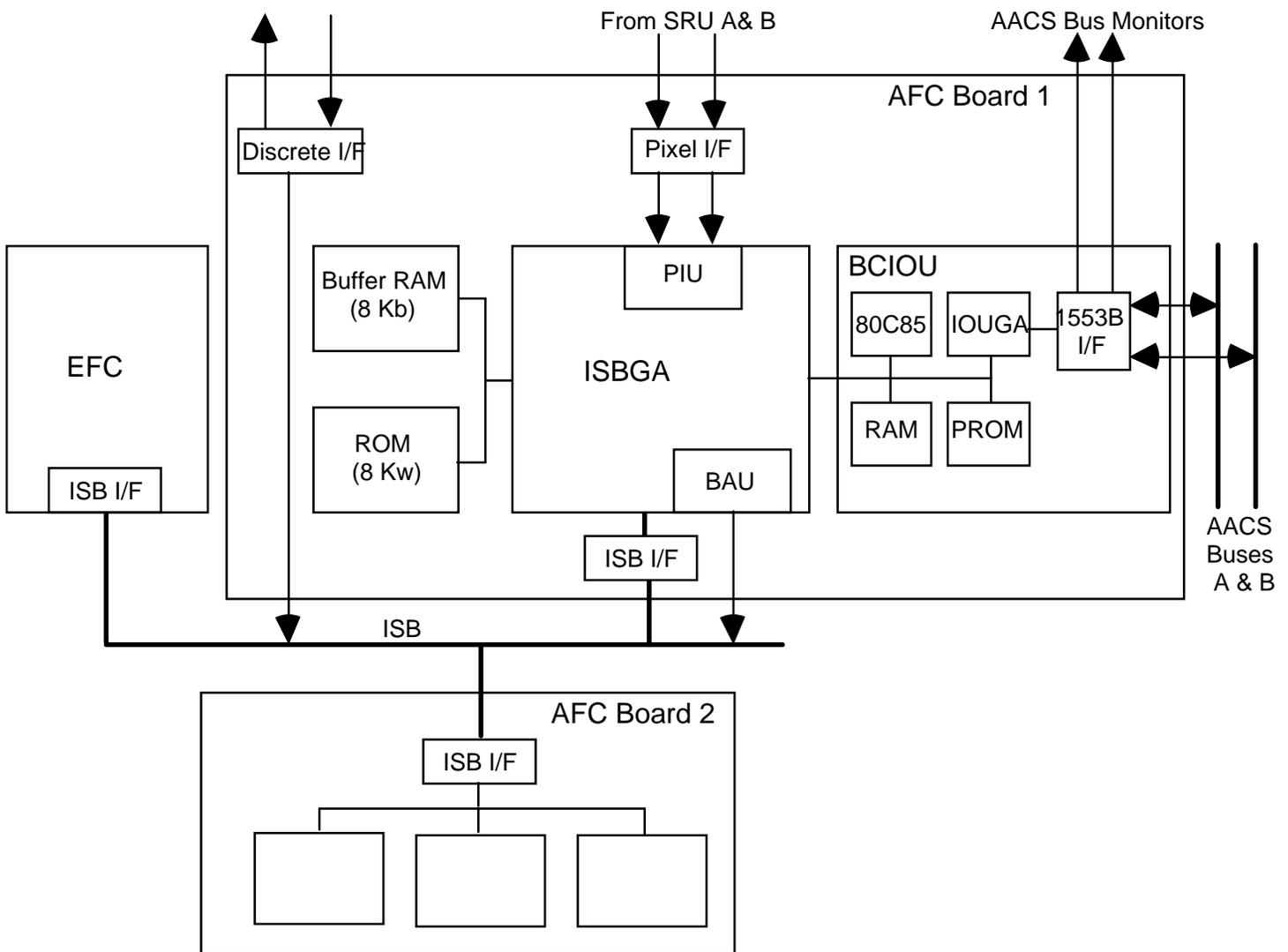


Figure 1-1 INTER-SUBASSEMBLY BUS GA IN ACS FLIGHT COMPUTER

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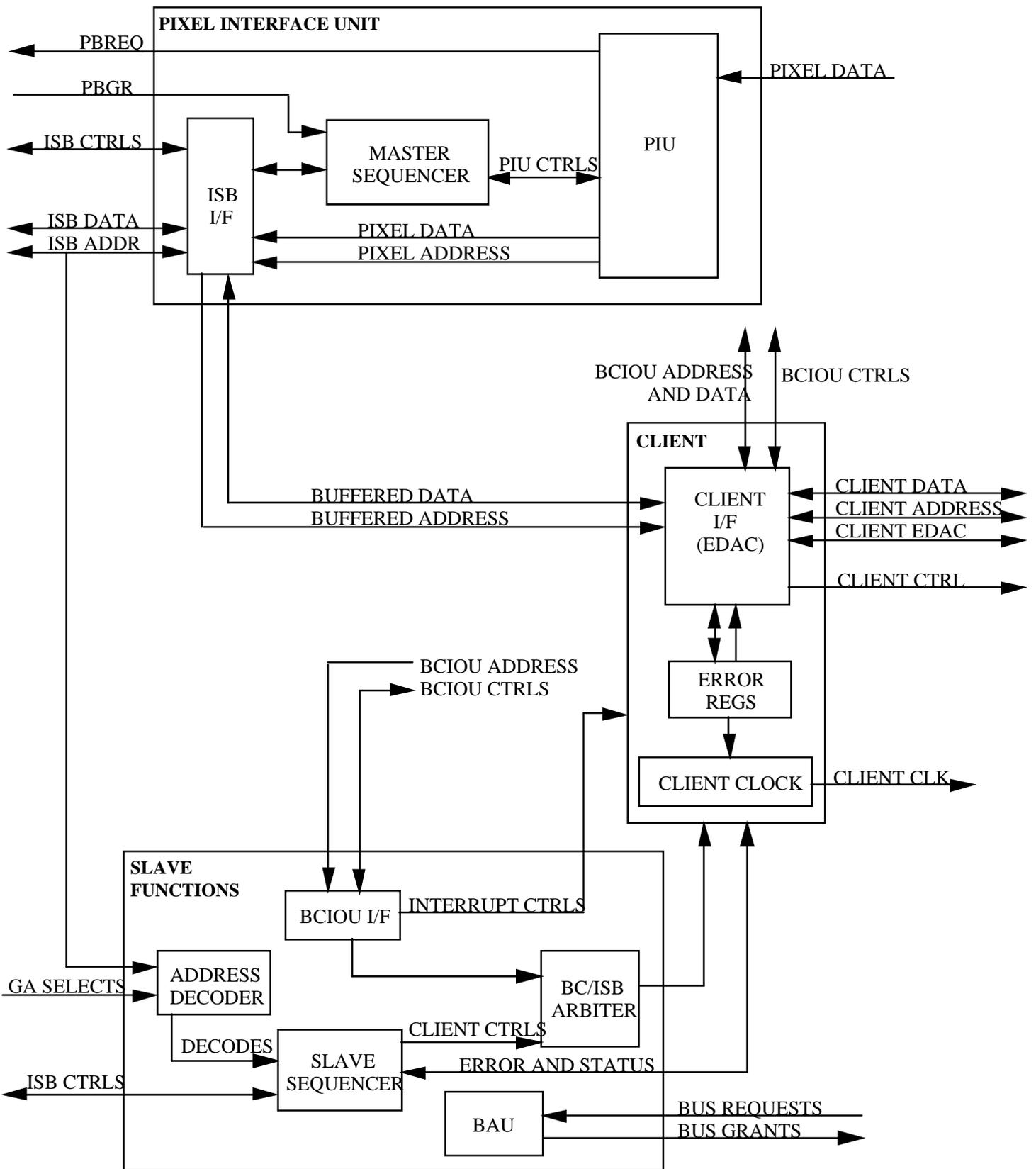


Figure 1-2 INTER-SUBASSEMBLY BUS GA FUNCTIONAL BLOCK DIAGRAM

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The figure below shows the significant modules of the ISBGA arranged hierarchically. The names in parentheses are the module names used in the gate array netlist.

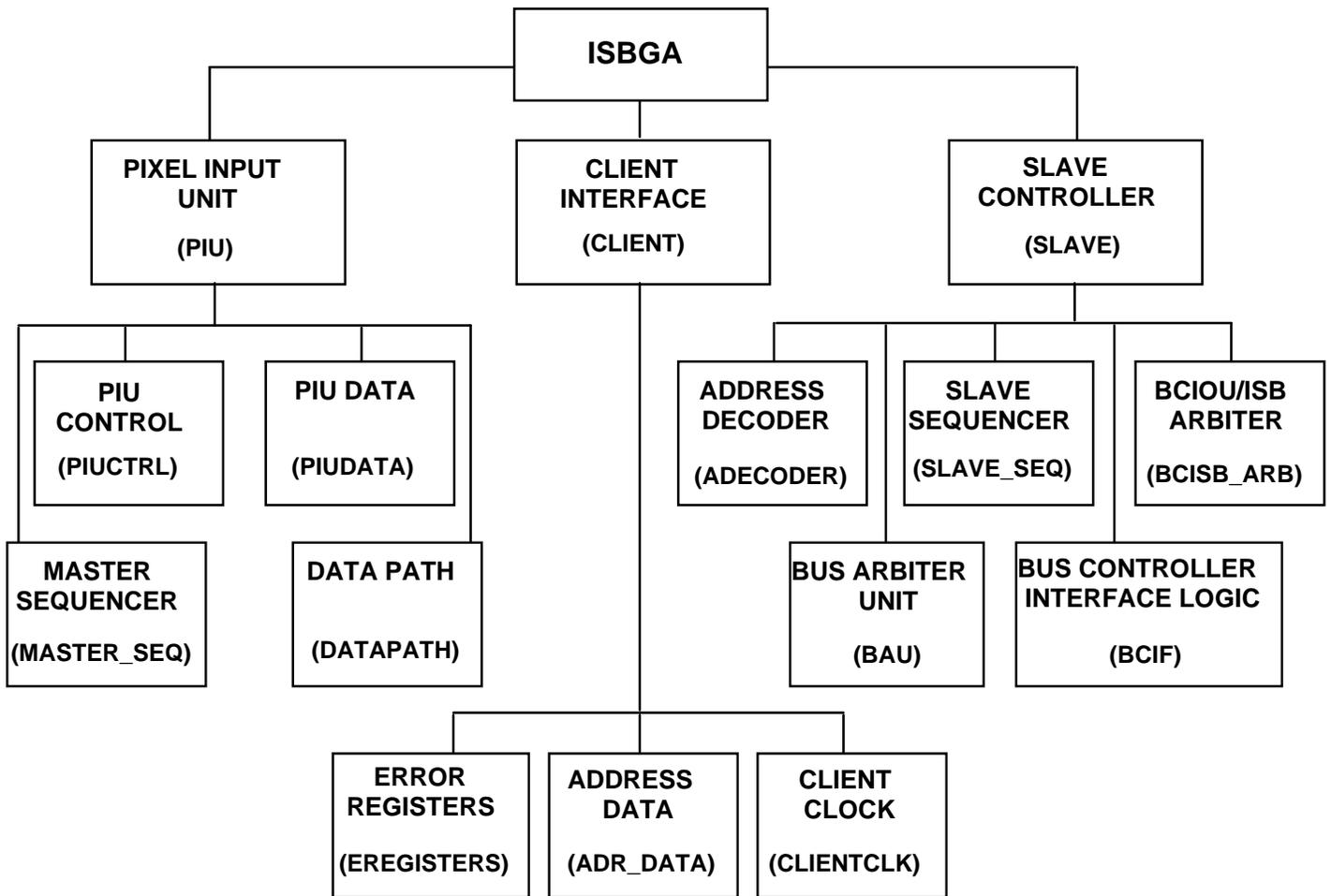
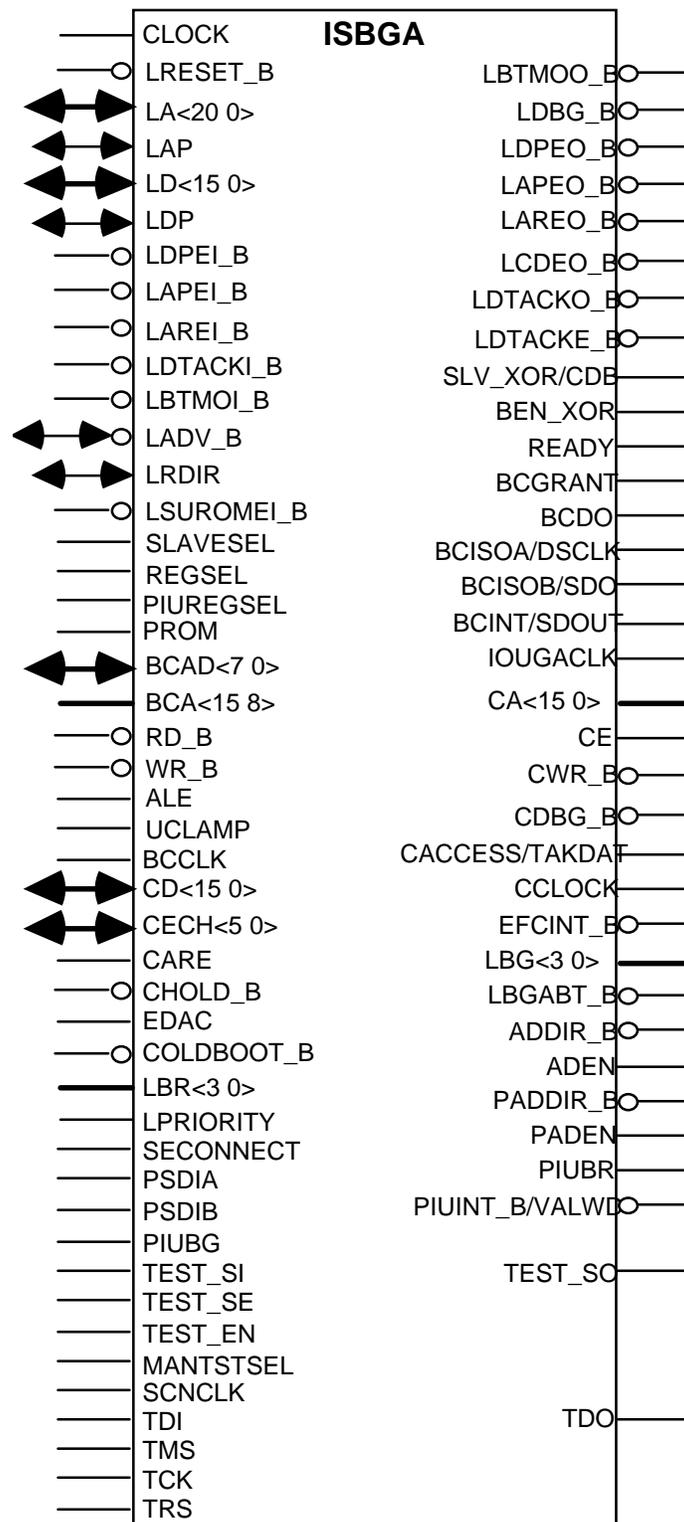


Figure 1-3 INTER-SUBASSEMBLY BUS GA MODULE DIAGRAM

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2. INTER-SUBASSEMBLY BUS GA SIGNAL DESIGNATIONS AND DESCRIPTIONS



NOTE: This figure shows the signal name designations of the chip, exclusive of power and ground. Bidirectional signals are indicated by arrows. All other signals on the left side of the symbol are inputs; those on the right side are outputs.

Figure 2-1 INTER-SUBASSEMBLY BUS GA SYMBOL

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The following table lists the ISBGA signals and their descriptions. Actual pin assignments are specified in section 6 of this drawing. Pad locations on the die, as shown in Table 6-1, are assigned in conjunction with the ASIC manufacturer during the layout phase in order to conform to the pin assignments and bonding rules. There are a total of 165 signal pins, including master reset and scan test pins. There are a total of 24 power and ground pins and 5 JTAG interface pins used for this ASIC.

Table 2-1 Signal Descriptions

Signal Name	Pin Number	Type	Drive ¹	I/O Macro Type ²	Module	Description
LA<20...0>	63...73, 76...85 (See Table 2-2)	I/O	AHZ	BCNC10	ISB	ISB Address: Input when ISBGA is Slave, output when ISBGA is the Bus Master through the PIU.
LAP	62	I/O	AHZ	BCNC10	ISB	ISB Address Parity Bit: Input when ISBGA is Slave and validated by Slave device. Generated by ISBGA when Bus Master through the PIU.
LD<15...0>	32...47 (See Table 2-2)	I/O	AHZ	BCNC10	ISB	ISB Data: Input for Slave writes, and output during Slave reads. Output only when ISBGA is Bus Master through PIU.
LDP	31	I/O	AHZ	BCNC10	ISB	ISB Data Parity Bit: Input for ISBGA Slave writes and validated by Slave device. Generated by ISBGA during Slave reads or Master writes through PIU.
LADV_B	52	I/O	ALZ	BCNC10	Master Seq. Slave Seq.	ISB Address Valid: Generated by Master Sequencer when ISB Address, Data and RDIR are valid on the ISB. Used by Slave Sequencer to initiate slave functions if ISBGA is selected device.
LRDIR	53	I/O	AHZ	BCNC10	Master Seq. Slave Seq.	ISB Read Direction: Generated by Master Sequencer when PIU is Bus Master. Since the PIU can only perform ISB writes, this signal will always be set to logic "0" during ISBGA Bus Master transactions. Used by Slave Sequencer when ISBGA is selected as slave device to determine read or write timing.
LDPEI_B	54	Input	AL	ICN10	Master Seq.	ISB Data Parity Error In: Generated by the Slave device when ISBGA is Bus Master through PIU. Sets error bit in ISB Register 0. Indicates that the Slave device received bad data on the ISB.
LAPEI_B	55	Input	AL	ICN10	Master Seq.	ISB Address Parity Error In: Generated by the Slave device when ISBGA is Bus Master through PIU. Sets error bit in ISB Register 0. Indicates that the Slave device received bad address bits on the ISB.
LAREI_B	56	Input	AL	ICN10	Master Seq.	ISB Address Range Error In: Generated by the Slave device when ISBGA is Bus Master through PIU. Sets error bit in ISB Register 0. Indicates that Slave device received address that was outside of its valid decode range.
LBTMOO_B	57	Output	AL	OCN40	Master Seq.	ISB Bus Time-out Out: Generated by Master Sequencer when DTACKI* is not received within 15 μ s from LADV_B being asserted.
LDTACKI_B	58	Input	AL	ICN10	Master Seq.	ISB Data Acknowledge In: Generated by current ISB Slave device. Used by master sequencer to indicate that the ISB write transaction is finished.
LDPEO_B	59	Output	AL	OCN40	Slave Seq.	ISB Data Parity Error Out: Generated by Slave when bad ISB data is detected during an ISB write. Sets error bit in ISB Register 3.

^{1, 2} See notes on last page of table.

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Table 2-1 Signal Descriptions (cont.)

Signal Name	Pin Number	Type	Drive ¹	I/O Macro Type ²	Module	Description
LAPEO_B	60	Output	AL	OCN40	Slave Seq.	ISB Address Parity Error Out: Generated by Slave when bad ISB address bits are detected during ISB reads or writes. Sets error bit in ISB Register 3.
LAREO_B	61	Output	AL	OCN40	Slave Seq.	ISB Address Range Error Out: Generated by Address Decoder whenever an unassigned register in the PIU or ISB Error Registers is addressed. Also generated if an out of range Client Address is requested. Sets error bit in ISB Register 3.
LCDEO_B	86	Output	AL	OCN40	Slave Seq.	ISB Corrected Data Error Out: Generated by Slave when a correctable data error is detected during an ISB read. The corrected data is placed on the ISB. Sets error bit in ISB Register 3.
LBTMOI_B	92	Input	AL	ICN10	Slave Seq.	ISB Bus Time-out In: Generated by current ISB master when Slave fails to assert DTACK within 15 μ s of LADV_B being asserted. Slave is reset to its idle state.
LDTACKO_B	93	Output	AL	OCN40	Slave Seq.	ISB Data Acknowledge Out: Generated by Slave to indicate that ISB write is completed, or ISB read data is valid.
LDTACKE_B	94	Output	AL	OCN40	Slave Seq.	Local Data Acknowledge Enable: Can be used to enable external 3-state driver for LDTACKO*.
LSUROMEI_B	95	Input	AL	ICN10	Slave Seq.	ISB Startup ROM Enable: Generated by EFC to indicate ROM reads of the first 64K ISB address space.
LDBG_B	96	Output	AL	OCN40	Slave Seq.	Local Data Bus Enable: Controls direction of Local Data bus transceivers for read/write operations.
LRESET_B	87	Input	AL	ICN10	All	WARMBOOT: Synchronous reset to ISB Gate Array.
CLOCK	17	Input	AH	ICN10	All	Global 12 MHz Gate Array Clock.
BCAD<7...0>	125...132 (See Table 2-2)	I/O	AHZ	BCNC10	BC I/F	BCIOU Multiplexed 80C85 Address Lower Byte and Bidirectional Data.
BCA<15...8>	107...114 (See Table 2-2)	Input	AH	ICN10	BC I/F	BCIOU 80C85 Address Upper Byte.
RD_B	105	Input	AL	ISN10	BC I/F	BCIOU 80C85 Read Enable.
WR_B	104	Input	AL	ISN10	BC I/F	BCIOU 80C85 Write Enable.
ALE	103	Input	AH	ISN10	BC I/F	BCIOU 80C85 Address Latch Enable: Used to latch lower address byte from multiplexed AD<7...0> bus.
READY	102	Output	AH	OCN40	BC I/F	BCIOU 80C85 Ready Line: Used for wait state generation.
BCDO	101	Output	AH	OCN40	BC I/F	BCIOU Data Direction.
UCLAMP	90	Input	AH	ICN10	BC I/F	IOU Gate Array UCLAMP signal: Indicates BCIOU is clamped or in reset state.
BCCLK	122	Input	AH	ISN10	BC I/F	BCIOU 2 MHz 80C85 processor clock.
BCISOA	133	Output	AH	OCN40	BC I/F	BCIOU Isolation from AACS Bus A.
DSCLK					Scan Test	Manchester Serial Data Clock: During scan test provides synthesized clock output from MANDEC macro for observability.

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^{1, 2} See notes on last page of table.

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Table 2-1 Signal Descriptions (cont.)

Signal Name	Pin Number	Type	Drive ¹	I/O Macro Type ²	Module	Description
BCISOB	134	Output	AH	OCN40	BC I/F	BCIOU Isolation from AACS Bus B.
SDO					Scan Test	Manchester Serial Data Output: During scan test provides serial data word output from MANDEC macro for observability.
BCINT	135	Output	AH	OCN40	BC I/F	BCIOU Maskable Interrupt.
SDOUT					Scan Test	Manchester Scan Data Output: During scan test provides scan data output from MANDEC macro for observability.
BCGRANT	106	Output	AH	OCN40	BC I/F	BCIOU Bus Grant: True when BCIOU is accessing the client bus.
IOUGACK	116	Output	AH	OCN40	BC I/F	System Clock: Buffered copy of the 12 MHz Gate Array clock.
CA<15...0>	187...194, 3...10 (See Table 2-2)	Output	AH	OCN40	Client I/F	Client Address Bus.
CD<15...0>	163...170, 173...180 (See Table 2-2)	I/O	AHZ	BCNC10	Client I/F	Client Data Bus.
CECH<5...0>	140...145 (See Table 2-2)	I/O	AHZ	BCNC10	Client I/F	Client Error Correction Bits.
CACCESS	186	Output	AH	OCN40	Client I/F	Client Access: Logic "1" when Client Bus is being addressed. Precedes CE by one clock cycle.
TAKDAT					Scan Test	Take Manchester Data: During scan test provides TAKDAT output from MANDEC macro for observability.
CE	185	Output	AH	OCN40	Client I/F	Client Enable: Indicates Slave transaction is taking place to the client interface.
CWR_B	184	Output	AL	OCN40	Client I/F	Client Write Strobe.
CDBG_B	183	Output	AL	OCN40	Client I/F	Client Data Bus Enable: Used for Client Data bus transceiver direction control.
CARE	182	Input	AH	ICN10	Client I/F	Client Address Range Error.
CHOLD_B	181	Input	AL	ICN10	Client I/F	Client Hold: Used to insert one wait state in current client transaction.
CCLOCK	150	Output	AH	OCN40	Client I/F	Client Clock: 1 μ s pulse with programmable period from 2 μ s to 65 ms (default = 15.63 ms).
EFCINT_B	30	Output	AL	OCN40	Client I/F	EFC Interrupt: Used to indicate ISB error, BCIOU clamp or BCIOU service request.
COLDBOOT_B	152	Input	AL	ICN10	Client I/F	COLDBOOT: Used to reset CCLOCK.
EDAC	153	Input	AH	ICN10	Client I/F	Error Detection and Correction Enable. This input is not resynchronized to CLOCK.
LBR<0>	11	Input	AH	ICN10	Bus Arbiter	Local Bus Request 0: Single cycle DMA.
LBR<1>	13	Input	AH	ICN10	Bus Arbiter	Local Bus Request 1: Single cycle DMA.
LBR<2>	19	Input	AH	ICN10	Bus Arbiter	Local Bus Request 2: Single cycle DMA, with priority to hold bus indefinitely.
LBR<3>	21	Input	AH	ICN10	Bus Arbiter	Local Bus Request 3: Multiple cycle DMA, intended for EFC.
LPRIORITY	28	Input	AH	ICN10	Bus Arbiter	Local Priority: Hold Bus Grant 2 indefinitely.

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^{1, 2} See notes on last page of table.

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Table 2-1 Signal Descriptions (cont.)

Signal Name	Pin Number	Type	Drive ¹	I/O Macro Type ²	Module	Description
SECONNECT	23	Input	AH	ICN10	Bus Arbiter	Support Equipment Connected: Enables LPRIORITY to hold Bus Grant 2.
LBG<0>	12	Output	AH	OCN40	Bus Arbiter	Local Bus Grant 0: Single cycle DMA.
LBG<1>	14	Output	AH	OCN40	Bus Arbiter	Local Bus Grant 1: Single cycle DMA.
LBG<2>	20	Output	AH	OCN40	Bus Arbiter	Local Bus Grant 2: Single cycle DMA, with priority to hold indefinitely.
LBG<3>	22	Output	AH	OCN40	Bus Arbiter	Local Bus Grant 3: Multiple cycle DMA, intended for EFC.
LBGABT_B	29	Output	AL	OCN40	Bus Arbiter	Local Bus Grant Abort: Used to force user of Bus Request 3 (multiple cycle DMA) off ISB.
ADDIR_B	27	Output	AL	OCN40	Bus Arbiter	Address Direction: Used to control direction pin of HCS245 transceiver for driving local addresses onto the ISB whenever the Bus Masters on LBR<0> or LBR<2> are active. When logic "0" indicates that Bus Masters on LBR<0> or LBR<2> are driving addresses on the ISB.
ADEN	26	Output	AH	OCN40	Bus Arbiter	Address Enable: Used to control enable pin of HCS245 transceiver for driving local addresses onto the ISB whenever the Bus Masters on LBR<0> or LBR<2> are active. Combined with ADDIR_B, creates break before make Local bus control.
PADDIR_B	16	Output	AL	OCN40	Bus Arbiter	Pixel Address Direction: Used to control direction pin of HCS245 transceiver for driving local addresses onto the ISB whenever the Bus Master on LBR<1> is active. When logic "0" indicates that Bus Master on LBR<1> is driving addresses on the ISB.
PADEN	15	Output	AH	OCN40	Bus Arbiter	Pixel Address Enable: Used to control enable pin of HCS245 transceiver for driving local addresses onto the ISB whenever the Bus Master on LBR<1> is active. Combined with PADDIR_B, creates break before make Pixel bus control.
PSDIA	154	Input	AH	ICN10	PIU	Pixel Serial Data In Bus A.
PSDIB	155	Input	AH	ICN10	PIU	Pixel Serial Data In Bus B.
PIUBR	156	Output	AH	OCN40	PIU	PIU Bus Request: Designed for a single cycle DMA bus request.
PIUBG	157	Input	AH	ICN10	PIU	PIU Bus Grant: From corresponding Bus Grant of Bus Arbiter.
PIUINT_B	158	Output	AL	OCN40	PIU	PIU Interrupt to EFC.
VALWD			AH		Scan Test	Valid Manchester Word: During scan test provides VALWD output from MANDEC macro for observability.
SLAVESEL	159	Input	AH	ICN10	Slave Seq.	Slave Access: Indicates current ISB access belongs to 64K ISB Gate Array address space.
REGSEL	160	Input	AH	ICN10	Slave Seq.	Register Select: Indicates current ISB access belongs to ISB Gate Array Error and Control Registers.
PIUREGSEL	161	Input	AH	ICN10	Slave Seq.	PIU Register Select: Indicates current ISB access belongs to ISB Gate Array PIU Registers.

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PROM	162	Input	AH	ICN10	Slave Seq.	PROM Enable: Enables SUROM use of the Client Bus. This signal is not resynchronized to CLOCK.
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^{1, 2} See notes on last page of table.

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Table 2-1 Signal Descriptions (cont.)

Signal Name	Pin Number	Type	Drive ¹	I/O Macro Type ²	Module	Description
SLV_XOR	91	Output	AH	OCN40	Slave Seq. BC I/F	Test output: Slave Sequencer Running or BCIF XOR Plane.
CDB					Scan Test	Test output: When MANTSTSEL is true, this is the MANDEC macro Command/Data Sync.
BEN_XOR	151	Output	AH	OCN40	Client I/F Slave PIU	Test output: Observability for EREG XOR Plane or 3-State Enable XOR Plane.
MANTSTSEL	89	Input	AH	ICN10	Scan Test	Manchester Test Select: Enables MANDEC macro scan test outputs (multiplexed on other output pins). Pull-down on board. ³
SCNCLK	88	Input	AH	ICN10	Scan Test	Manchester Scan Clock: MANDEC macro scan test input clock. Pull-up on board. ³
TEST_SE	137	Input	AH	ICN10	Scan Test	Manchester Scan Test Enable: Enables test of MANDEC macro. Pull-down on board. ³
TEST_SI	138	Input	AH	ICN10	Scan Test	Scan Test Serial Data In. Pull-down on board. ³
TEST_EN	136	Input	AH	ICN10	Scan Test	Scan Test Enable. Pull-down on board. ³
TEST_SO	139	Output	AH	OCN40	Scan Test	Scan Test Serial Data Out
TCK	121	Input	AH	ITTCK	JTAG	JTAG TAP Controller Clock. Pull-up on board. ³
TMS	120	Input	AH	ITTMS	JTAG	JTAG TAP Controller Mode Select. Pull-down on board. ³
TDI	119	Input	AH	ITTDI	JTAG	JTAG TAP Serial Input Data. Pull-up on board. ³
TDO	118	Output	AH	O4TDO	JTAG	JTAG TAP Serial Output Data
TRS	117	Input	AH	ITRS19	JTAG	JTAG TAP Reset. Pull-down on board. ³

¹ Drive may be active high (AH), active low (AL), active high 3-state (AHZ), etc.

² **I/O macros** (Refer to DC characteristics table in section 5.4 for drive capabilities of output buffers.):

- ICN10 CMOS input buffer
- ISN10 Schmitt trigger input buffer
- OCN40 CMOS output buffer, slow-slew
- BCNC10 Bidirectional CMOS input/output buffer
- ITTCK TTL-level input buffer
- ITTMS TTL-level input buffer with active pull-up
- ITTDI TTL-level input buffer with active pull-up
- O4TDO TTL-level output buffer
- ITRS19 TTL-level input buffer

³ Pull-up and pull-down information supplied to assure inactivation of gate array test circuitry on flight board.

Table 2-2 Bus Pin Assignments

Bus Signal	Pin No.								
LA<20>	72	LD<15>	32	BCA<15>	107	CA<15>	193	CD<15>	163
LA<19>	70	LD<14>	33	BCA<14>	108	CA<14>	191	CD<14>	164
LA<18>	68	LD<13>	34	BCA<13>	109	CA<13>	189	CD<13>	165
LA<17>	66	LD<12>	35	BCA<12>	110	CA<12>	187	CD<12>	166
LA<16>	64	LD<11>	36	BCA<11>	111	CA<11>	4	CD<11>	167
LA<15>	77	LD<10>	37	BCA<10>	112	CA<10>	6	CD<10>	168
LA<14>	79	LD<9>	38	BCA<9>	113	CA<9>	8	CD<9>	169
LA<13>	81	LD<8>	39	BCA<8>	114	CA<8>	10	CD<8>	170
LA<12>	83	LD<7>	40	BCAD<7>	125	CA<7>	9	CD<7>	173
LA<11>	85	LD<6>	41	BCAD<6>	126	CA<6>	7	CD<6>	174
LA<10>	84	LD<5>	42	BCAD<5>	127	CA<5>	5	CD<5>	175
LA<9>	82	LD<4>	43	BCAD<4>	128	CA<4>	3	CD<4>	176
LA<8>	80	LD<3>	44	BCAD<3>	129	CA<3>	188	CD<3>	177
LA<7>	78	LD<2>	45	BCAD<2>	130	CA<2>	190	CD<2>	178
LA<6>	76	LD<1>	46	BCAD<1>	131	CA<1>	192	CD<1>	179
LA<5>	63	LD<0>	47	BCAD<0>	132	CA<0>	194	CD<0>	180
LA<4>	65							CECH<5>	140
LA<3>	67							CECH<4>	141
LA<2>	69							CECH<3>	142
LA<1>	71							CECH<2>	143
LA<0>	73							CECH<1>	144
								CECH<0>	145

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3. FUNCTIONAL DESCRIPTION

DEFINITIONS

An ISBGA client is defined as a slave device that is accessible by ISB master devices or the BCIU through the ISB Gate Array.

AACS	Attitude and Articulation Control Subsystem
AACSE	AACS Control Electronics
A/B	AACS Bus Select
AFC	AACS Flight Computer
BAU	Bus Arbiter Unit
BCIF	Bus Controller Interface
BCIOU	Bus Controller Input Output Unit
CCD	Charge Coupled Device
DMA	Direct Memory Access
EDAC	Error Detection and Correction
EFC	Engineering Flight Computer
F. E.	Falling Edge
GA	Gate Array
IOU	Input Output Unit
ISB	Inter-Subassembly Bus
ISBGA	Inter-Subassembly Bus Gate Array
I/F	Interface
MANDEC	Manchester Decoder Macro
PIU	Pixel Input Unit
RTIOU	Remote Terminal Input Output Unit
R. E.	Rising Edge
SE	Support Equipment
SRU	Stellar Reference Unit
SUROM	Start-Up Read-Only Memory
TAP	Test Access Port
T/R	Transmit/Receive

3.1 ISBGA Functional Blocks

- Bus Controller Interface
- Slave Sequencer
- BCIU/ISB Arbiter
- Bus Arbiter Unit (BAU)
- Address Decoder
- Client Interface Address/Data
- Error Detection and Correction (EDAC) Unit
- Error Registers
- Master Sequencer
- Pixel Input Unit (PIU)

3.2 Interface Requirements

The following are the requirements placed on the ISBGA which are specific to the application of the ISBGA as the interface for SUROM, BCIU, PIU, BAU.

3.2.1 SUROM Interface

3.2.1.1 The ISBGA shall provide slave, read only access to the SUROM.

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- 3.2.1.2 The ISBGA shall provide address, data and enable signals to allow for up to 64K of 16 bit SUROM with 6 bit EDAC for a total of 22 bits to be accessed via the ISB.
- 3.2.1.3 Decode of individual SUROM chip selects will be done external to the ISB Gate Array through the Client Interface.
- 3.2.1.4 In the event of an ISB detected error (DPE — Data Parity Error, APE — Address Parity Error, Local ARE — Local Address Range Error, CDE — Corrected Data Error, UCDE — Uncorrected Data Error) during a slave read of the SUROM the ISBGA shall:
1. Capture the ISB Address, ISB Data and Client EDAC check bits in its error registers.
 2. Set SDPE, SAPE, SARE, SCDE or SUCDE as required in ISB error register 3. If SUCDE is detected, then bad data parity shall be asserted on the ISB.
 3. Set LDPEO_B, LAPEO_B, LAREO_B or LCDEO_B as required.
 4. In the event of a slave detected error, no interrupt shall be asserted. The current Bus Master is responsible for monitoring ISB error conditions.
- 3.2.1.5 The ISBGA shall generate a parity bit for the SUROM data and supply this bit on the ISB in concert with the SUROM data.
- 3.2.1.6 The ISBGA shall respond to ISB SUROM accesses on the basis of LSUROME, LRDIR and the ISB address as follows:

<u>LSUROME</u>	<u>LRDIR</u>	<u>Address</u>	<u>Response</u>
True	True	000000-00FFFF	Provide requested ROM data
True	False	000000-00FFFF	No Response (write belongs to EFC RAM)
False	True	000000-00FFFF	No Response (read belongs to EFC RAM)
False	False	000000-00FFFF	No Response (write belongs to EFC RAM)

- 3.2.1.7 The ISBGA shall respond to aliased ISB SUROM accesses on the basis of SLAVESEL, LRDIR and the ISB address as follows:

<u>SLAVESEL</u>	<u>LRDIR</u>	<u>Address</u>	<u>Response</u>
True	True	xx0000-xxFFFF	Provide requested ROM data
True	False	xx0000-xxFFFF	No Response

xx = decoded externally, selected by signal SLAVESEL

3.2.2 Bus Controller Interface (BCIF)

- 3.2.2.1 The ISBGA shall provide an arbitrated dual port interface to an 8K by 8 bit RAM. The two ports shall be the ISB and a BCIU (Bus Controller Input Output Unit). The 8K by 8 bit RAM shall be considered as part of the Client Interface.
- 3.2.2.2 The BCIU shall perform 80C85 microprocessor initiated reads and writes to the Client Interface only.
- 3.2.2.3 The ISBGA shall not require the BCIU to contain other than standard RTIU electronic hardware.
- 3.2.2.4 The ISBGA interface to the BCIU shall follow standard 80C85 memory interface protocol as defined in the Harris Rad-Hard/Hi-Rel data book.
- 3.2.2.5 The ISBGA interface to the BCIU shall use the following standard 80C85 signals to support access to the Client Interface: A<15...8>, AD<7...0>, RDB, WRB, ALE, READY.
- 3.2.2.6 The ISBGA shall provide an internal mechanism to latch address bits 0 through 7 and concatenate them with address bits 8 through 15 to provide a 16 bit address on the client address lines.
- 3.2.2.7 The ISBGA shall arbitrate between ISB and BCIU access on a round robin basis.

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- 3.2.2.8 In the event that an in process EFC access prevents a BCIOU access from completing within the 80C85 time allowance, the ISBGA shall de-assert READY according to the 80C85 timing criterion in order to halt the 80C85 until the RAM is available.
- 3.2.2.9 In the event that an in process BCIOU access prevents an ISB access from immediately completing, the ISBGA shall hold off asserting LDTACKO_B until the BCIOU access is complete and the pending ISB access has reached the appropriate point for asserting LDTACKO_B.
- 3.2.2.10 The ISBGA shall hold off asserting LDTACKO_B in an ISB/IOU arbitration conflict for at most 2 μ s longer than in a non conflicting access.
- 3.2.2.11 The ISBGA shall decode A<15...8> and AD<7...0> such that the Client Interface maps into BCIOU address space 1000 to 2FFD. Two locations, 2FFE and 2FFF, will not be accessible by the BCIOU.
- 3.2.2.12 The ISBGA shall decode A<15...8> and AD<7...0> such that a BCIOU read or write to BCIOU address 2FFF shall set the EFCI (Bus controller EFC Interrupt) bit in ISBGA Register 0. Setting EFCI shall cause an EFC interrupt.
- 3.2.2.13 The ISBGA shall decode A<15...8> and AD<7...0> such that a BCIOU read or write to BCIOU address 2FFE shall clear the BCI bit in ISBGA error register 4.
- 3.2.2.14 The BCIOU shall be unable to read the ISBGA error registers.

3.2.3 Pixel Input Unit (PIU)

- 3.2.3.1 The ISBGA shall provide a master and slave interface to the ISB for the PIU. The master interface shall be for PIU initiated pixel transfers. The slave interface shall be for PIU register reads and writes from the ISB.
- 3.2.3.2 The PIU shall be able to write pixel data to all ISB addresses via the ISBGA except for its own internal registers. Attempted pixel writes to PIU registers shall cause an ARE on the ISB.
- 3.2.3.3 Data from the Stellar Reference Unit (SRU) to the PIU shall be received serially. This data stream shall be Manchester encoded (self-clocking and asynchronous). Pixel data written across the ISB shall be in a parallel format as described in ES515831.
- 3.2.3.4 The PIU received data shall be 12 bits of pixel data and two status bits — End of Line (EOL) and End of Data (EOD). Pixel data written across the ISB shall consist of 12 bits of pixel data, three status bits — EOD, EOL and Manchester Error, and one bit forced to logic “0”. EOL shall indicate the last word of the current CCD line. EOD shall indicate the last word of a requested pixel frame.
- 3.2.3.5 The PIU controller shall transfer pixels across the ISB in a manner that is intended to store the pixels in a slave device in the same order as they are read from the SRU. If a received pixel from the SRU cannot be transferred, then the corresponding location in the slave device will be skipped.
- 3.2.3.6 The ISBGA shall generate a parity bit for PIU produced address and data and supply this bit on the ISB in concert with the PIU data and address.
- 3.2.3.7 The ISBGA shall support the PIU as an ISB Master by responding to ISB errors (DPE, APE, ARE and BTMO — Bus Time-out) from any slave device as follows:
 1. Capturing the current ISB Address, ISB Data and parity bits in its error registers.
 2. Setting MDPE, MAPE, MARE or MBTMO as required in ISB error register 0.
 3. Setting EFCI in ISB error register 0 which asserts an EFC interrupt.

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- 3.2.3.8 The ISBGA shall support the PIU as an ISB Master by generating LBTMOO_B in the event an addressed slave fails to assert the ISB signal DTACK* within 15 μ s after the ISB signal ADV* is asserted.
- 3.2.3.9 In the event of an ISB detected error (DPE, APE or Local ARE) during a PIU register read or write function, the ISBGA shall:
1. Capture the ISB Address, ISB Data and parity bits in its error registers.
 2. Set SDPE, SAPE or SARE as required in ISB error register 3.
 3. Set LDPEO_B, LAPEO_B or LAREO_B as required.
 4. In the event of a slave detected error, no interrupt shall be asserted. The current Bus Master is responsible for monitoring ISB error conditions.

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3.2.4 Client Interface

- 3.2.4.1 The ISB Gate Array shall provide an interface to allow slave access to client devices through the ISB.
- 3.2.4.2 The client interface shall be such that slave devices need only provide address decode and buffering of ISBGA signals. All critical timing signals for slave interactions shall be provided by the ISBGA.
- 3.2.4.3 The slave interface to the ISBGA shall function independent of PIU master requests.
- 3.2.4.4 The ISBGA shall always control the direction of data flow on the client data bus. The data bus three-state drivers resident within the client will be directly controlled by the CDBG_B signal with no decoding within the client required or allowed. The ISBGA shall guarantee that no overlap of bus drivers occurs and that no bus remains without a driver for more than 100 ns.
- 3.2.4.5 It is the responsibility of all client slave devices to provide a CARE (Client Address Range Error) signal to the ISBGA in the event the address presented to the client is not in the client's decoded address space.
- 3.2.4.6 All ISBGA generated client signals except CDBG_B shall change on the rising edge of system clock (CLOCK). CDBG_B asserts with the falling edge of CLOCK and deasserts with the rising edge of CLOCK.
- 3.2.4.7 All client generated signals shall change state on the falling edge of CLOCK.
- 3.2.4.8 The ISBGA shall contain EDAC circuitry to provide for double bit data error detection and single bit error correction on the Client Interface.
- 3.2.4.9 In the event of an ISB detected error (DPE, APE, ARE, CDE or UCDE) during a slave read or write of the Client Interface, the ISBGA shall:
 - 1. Capture the ISB Address, ISB Data and Client EDAC check bits in its error registers.
 - 2. Set SDPE, SAPE, SARE, SCDE or SUCDE as required in ISB error register 3. If SUCDE is detected, then bad data parity shall be asserted on the ISB.
 - 3. Set LDPEO_B, LAPEO_B, LAREO_B or LCDEO_B as required.
 - 4. In the event of a slave detected error, no interrupt shall be asserted. The current Bus Master is responsible for monitoring ISB error conditions.
- 3.2.4.10 The ISBGA shall provide a general purpose programmable clock for the Client Interface. The clock pulse width shall be 1 μ s and the period shall be programmable from 2 μ s to 64 ms. At reset, the clock shall be programmed to 15.63 ms. The clock shall be inactive "low" during Coldboot.

3.2.5 Bus Arbiter Unit (BAU)

- 3.2.5.1 The Bus Arbitration Unit shall arbitrate ISB mastership for up to 4 bus masters.
- 3.2.5.2 The BAU shall provide a bus request and bus grant for each bus master. The bus requests shall be prioritized, with LBR<0> as highest priority and LBR<3> as lowest priority.
- 3.2.5.3 The BAU shall provide a signal (LPRIORITY) that, when asserted, will prevent any other bus masters except LBR<2> from being granted the ISB. This is provided to allow the SE uninterrupted control over the ISB for loading memory and debugging.
- 3.2.5.4 The lowest priority bus request (LBR<3>), when granted, shall remain granted until another bus master requests ISB mastership or LBR<3> deasserts. The BAU shall provide a signal (LBGABT_B) to indicate that another bus master is requesting ISB mastership.

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3.2.5.5 The bus masters assigned to LBR<0>, LBR<1> and LBR<2> shall perform single cycle ISB transactions only. These masters must arbitrate for the bus for each transaction.

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3.3 ISBGA Register Descriptions

Reading or writing undefined register spaces in either the ISB Error and Control Registers, or the PIU Registers will cause an address range error to be generated. The ISB address range error is decoded by the client interface, and the PIU address range error is decoded by the PIU Controller. All register bits are reset to a "0" value unless otherwise stated.

Table 3-1 ISB Registers

#	ISB Address	Register Name	Type	Description
R0	REGSEL&00	ISBINT	R/W	ISB Error Interrupts, BCIU Service Interrupt and ISB Error Address MSW
R1	REGSEL&01	ISBADRLSW	R	ISB Error Address LSW
R2	REGSEL&02	ISBDATA	R	ISB Error Data
R3	REGSEL&03	ISBEDAC	R	ISB Error EDAC Bits
R4	REGSEL&04	BCINT	W	Interrupt from EFC to BCIU
R5	REGSEL&05	ERRCNT	R/W	ISB Error Count and BCIU Isolation Bits
R6	REGSEL&06	INTMSKS	R/W	ISB Error Interrupt Masks for Register 0
R7	REGSEL&07	CLKCNT	R/W	Client Clock Count period
n/a	REGSEL&08 through FF	unassigned	n/a	Address Range Error
P0	PIUREGSEL&00	STADR1LSW	R/W	PIU Start Address 1 LSW
P1	PIUREGSEL&01	STADR1MSW	R/W	PIU Start Address 1 MSW
P2	PIUREGSEL&02	ENDADR1LSW	R/W	PIU End Address 1 LSB
P3	PIUREGSEL&03	ENDADR1MSW	R/W	PIU End Address 1 MSW
P4	PIUREGSEL&04	STADR2LSW	R/W	PIU Start Address 2 LSW
P5	PIUREGSEL&05	STADR2MSW	R/W	PIU Start Address 2 MSW
P6	PIUREGSEL&06	ENDADR2LSW	R/W	PIU End Address 2 LSW
P7	PIUREGSEL&07	ENDADR2MSW	R/W	PIU End Address 2 MSW
P8	PIUREGSEL&08	ADRCNTLSW	R	PIU Address Count LSW
P9	PIUREGSEL&09	ADRCNTMSW	R	PIU Address Count MSW
P10	PIUREGSEL&0A	ERROR/STATUS	R/W	PIU Error and Status
P11	PIUREGSEL&0B	COMMAND	R/W	PIU Command Bits
n/a	PIUREGSEL&0C through FF	unassigned	n/a	Address Range Error

3.3.1 ISB Error and Status Register List

Table 3-2 R0: ISB Error Interrupts, BCIU Service Interrupt and ISB Address MSW

HBit #	SBit #	Type	Description
4:0	15:11	R	ISB Address Bits MSW (Bits 20:16) when ISB Error occurred.
5	10	R	ISB Data Parity Error state when ISB Error occurred.
6	9	R	ISB Address Parity Error state when ISB Error occurred.
7:8	8:7	n/a	Unused bits: will read 0.
9	6	R	UCLAMP Interrupt: occurs whenever BCIU is clamped or held in its reset state.
10	5	R	Master Bus Time-out Interrupt: occurs whenever PIU is bus master and active slave has not asserted LDTACKI_B within 15 μ s of LADV_B active.
11	4	R	Master Address Range Error Interrupt: occurs whenever PIU is bus master and active slave has indicated access to an undefined address space.
12	3	R	Master Data Parity Error Interrupt: occurs whenever PIU is bus master and active slave has asserted ISB Data Parity Error signal.
13	2	R	Master Address Parity Error Interrupt: occurs whenever PIU is bus master and active slave has asserted ISB Address Parity Error signal.
14	1	R/W	Writable by BCIU only: BCIU writes to address 2FFF hex in BCIU address space to set this bit and request EFC service.
15	0	R	EFC Interrupt State: Indicates when the EFC Interrupt signal is set.

All bits are cleared to "0" by write to Register 0 (data is don't care).

Table 3-3 R1: ISB Error Address LSW

HBit #	SBit #	Type	Description
15:0	0:15	R	ISB Address Bits LSW (Bits 15:0) when ISB Error occurred. Cleared by any write to R0.

Table 3-4 R2: ISB Error Data

HBit #	SBit #	Type	Description
15:0	0:15	R	ISB Data Bits (Bits 15:0) when ISB Error occurred. Cleared by any write to R0.

Table 3-5 R3: ISB Slave Errors and EDAC Bits

HBit #	SBit #	Type	Description
5:0	10:15	R	ISB EDAC Bits when ISB Error occurred.
10:6	5:9	n/a	Unused bits: will read "0".
11	4	R	Slave Uncorrected Data Error: set to "1" whenever ISB Gate Array is the active slave device and an uncorrectable data error was detected.
12	3	R	Slave Corrected Data Error: set to "1" whenever ISB Gate Array is the active slave device and a corrected data error occurred.
13	2	R	Slave Address Range Error: set to "1" whenever ISB Gate Array is the active slave device and the current ISB transaction is to an undefined address space.
14	1	R	Slave Data Parity Error: set to "1" whenever ISB Gate Array is the active slave device and a data parity error is detected during an ISB write.
15	0	R	Slave Address Parity Error: set to "1" whenever ISB Gate Array is the active slave device and an address parity error is detected.

All bits are cleared to "0" on any write to R0 (data is don't care).

Table 3-6 R4: EFC Interrupt to BCIOU

HBit #	SBit #	Type	Description
14:0	1:15	n/a	Unused bits: will read "0".
15	0	R/W	EFC Interrupt to BCIOU: Set to "1" whenever register is addressed during an ISB write transaction. Cleared to "0" by BCIOU when BCIOU writes to address 2FFE hex in BCIOU address space.

Table 3-7 R5: Error Count and BCIOU Isolation

HBit #	SBit #	Type	Description
3:0	12:15	R	ISB Error Count: Whenever an ISB error occurs, R0 through R3 latch the error conditions. Subsequent ISB errors will not relatch R0 through R3, but will increment the error count to a maximum count of 15. Cleared by any write to R0 (data is don't care).
4	11	R/W	BCIOU Isolation from AACS Bus A
5	10	R/W	BCIOU Isolation from AACS Bus B.
15:6	0:9	R/W	Unassigned bits.

Table 3-8 R6: ISB Error Interrupt Mask Bits

HBit #	SBit #	Type	Description
8:0	5:15	R/W	Unassigned bits.
9	6	R/W	UCLAMP Interrupt Mask.
10	5	R/W	Master Bus Time-out Interrupt Mask.
11	4	R/W	Master Address Range Error Interrupt Mask.
12	3	R/W	Master Data Parity Error Interrupt Mask.
13	2	R/W	Master Address Parity Error Interrupt Mask.
15:14	0:1	R/W	Unassigned bits.

Table 3-9 R7: Client Clock Count Period

HBit #	SBit #	Type	Description
15:0	0:15	R/W	Count period for 1 μ s Client pulse: Adjustable from 2 μ s to 65 ms period. If count is written with 0000 hex, the output signal will be forced to "1". Reset to 3D09 hex to provide a 15.63 ms period (for Fault Detection Reset Logic).

3.3.2 PIU Register List

Table 3-10 P0: Start Address 1 LSW

HBit #	SBit #	Type	Description
15:0	0:15	R/W	Start address LSW for PIU writes to buffer 1 in ISB address space.

Table 3-11 P1: Start Address 1 MSW

HBit #	SBit #	Type	Description
4:0	11:15	R/W	Start address MSW for PIU writes to buffer 1 in ISB address space.
15:5	0:10	n/a	Unassigned bits: will read "0"

Table 3-12 P2: End Address 1 LSW

HBit #	SBit #	Type	Description
15:0	0:15	R/W	End address LSW for PIU writes to buffer 1 in ISB address space.

Table 3-13 P3: End Address 1 MSW

HBit #	SBit #	Type	Description
4:0	11:15	R/W	End address MSW for PIU writes to buffer 1 in ISB address space.
15:5	0:10	n/a	Unassigned bits: will read "0"

Table 3-14 P4: Start Address 2 LSW

HBit #	SBit #	Type	Description
15:0	0:15	R/W	Start address LSW for PIU writes to buffer 2 in ISB address space.

Table 3-15 P5: Start Address 2 MSW

HBit #	SBit #	Type	Description
4:0	11:15	R/W	Start address MSW for PIU writes to buffer 2 in ISB address space.
15:5	0:10	n/a	Unassigned bits: will read "0"

Table 3-16 P6: End Address 2 LSW

HBit #	SBit #	Type	Description
15:0	0:15	R/W	End address LSW for PIU writes to buffer 2 in ISB address space.

Table 3-17 P7: End Address 2 MSW

HBit #	SBit #	Type	Description
4:0	11:15	R/W	End address MSW for PIU writes to buffer 2 in ISB address space.
15:5	0:10	n/a	Unassigned bits: will read "0"

Table 3-18 P8: Current Address Position LSW

HBit #	SBit #	Type	Description
15:0	0:15	R	When read, indicates address position (LSW) for current pixel word transfer.

Table 3-19 P9: Current Address Position MSW

HBit #	SBit #	Type	Description
4:0	11:15	R	When read, indicates address position (MSW) for current pixel word transfer.
15:5	0:10	n/a	Unassigned bits: will read "0"

Table 3-20 P10: Error and Status Register

HBit #	SBit #	Type	Description
0	15	R	Manchester Data Error occurred while buffer 1 was active. Generates interrupt to EFC if not masked.
1	14	R	End of Line occurred while buffer 1 was active. Generates interrupt to EFC if not masked.
2	13	R	End of Data occurred while buffer 1 was active. Generates interrupt to EFC if not masked.
3	12	R	Buffer 1 Full. Is set to "1" whenever the end address of buffer 1 is reached. Generates interrupt to EFC if not masked.
4	11	R	Buffer 1 Skip Error: Is set to "1" whenever a pixel has not been successfully transferred over the ISB before a new pixel has come in while buffer 1 was active.
5	10	R	ENDAD no EOD: Is set to "1" whenever the end address of buffer 1 is reached, but the EOD status was not in the last pixel.
6	9	R	EOD no ENDAD: Is set to "1" whenever an EOD status is received in a pixel, but buffer 1 is not at its end address.
7	8	R	Buffer 1 Active. Set to "1" by PIU Controller whenever buffer 1 is being used. Set to "0" by PIU Controller when buffer 1 is full.
8	7	R	Manchester Data Error occurred while buffer 2 was active. Generates interrupt to EFC if not masked.
9	6	R	End of Line occurred while buffer 2 was active. Generates interrupt to EFC if not masked.
10	5	R	End of Data occurred while buffer 2 was active. Generates interrupt to EFC if not masked.
11	4	R	Buffer 2 Full. Is set to "1" whenever the end address of buffer 2 is reached. Generates interrupt to EFC if not masked.
12	3	R	Buffer 2 Skip Error: Is set to "1" whenever a pixel has not been successfully transferred over the ISB before a new pixel has come in while buffer 2 was active.
13	2	R	ENDAD no EOD: Is set to "1" whenever the end address of buffer 2 is reached, but the EOD status was not in the last pixel.
14	1	R	EOD no ENDAD: Is set to "1" whenever an EOD status is received in a pixel, but buffer 2 is not at its end address.
15	0	R	Buffer 2 Active. Set to "1" by PIU Controller whenever buffer 2 is being used. Set to "0" by PIU Controller when buffer 2 is full.

Write to P10 (data is don't care) clears HBits 0 through 6, reloads HBit 7, clears HBits 8 through 14 and reloads HBit 15.

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Table 3-21 P11: Command Register

HBit #	SBit #	Type	Description
0	15	R/W	SRU Interface Select A or B: set to "0" to select interface A.
1	14	R/W	Freeze Count: used to hold copy of current address count so that ISB master may read without being updated in between.
2	13	R/W	ABORT: set to "1" to force PIU Controller to return to the ready state.
3	12	R/W	Enable Buffer 1: set to "1" to allow PIU to start using pixel buffer 1 starting at start address 1.
4	11	R/W	Enable Buffer 2: set to "1" to allow PIU to start using pixel buffer 2 starting at start address 2.
5	10	R/W	Manchester Data Error Interrupt Mask.
6	9	R/W	End of Line Interrupt Mask.
7	8	R/W	End of Data Interrupt Mask.
8	7	R/W	Buffer 1 Full Interrupt Mask.
9	6	R/W	Buffer 2 Full Interrupt Mask.
10	5	R/W	Disable Manchester Data Error Status: when set to "1" will prevent Manchester Data Error status from being stored with the pixel word.
11	4	R/W	Disable End of Line Status: when set to "1" will prevent EOL status from being written with the pixel word.
12	3	R/W	Disable End of Data Status: when set to "1" will prevent EOD status from being written with the pixel word.
13	2	R/W	Mask ISB Address Bit 20: when set to "1" will prevent PIU from accessing the upper 1 Mb ISB address space (User I/O space).
15:14	0:1	R/W	Unassigned bits.

3.4 Worst case timing specifications and timing diagrams

Worst case timing parameters are derived from the "Slow Simulation" (worst case condition: +125°C, +4.5 V, worst process and radiation condition). For sequential elements, the maximum setup time is 25 ns and the minimum hold time is 10 ns assuming 12.5 MHz maximum chip operating frequency with 60%-40% duty cycle. Refer to section 5.5 on sheet 33 under "AC Characteristics" for the AC parameters the Manufacturer will test for. The following timing diagrams are provided for user reference to understand various cycles of this gate array.

Figure 3-1 ISB TIMING

ISB Arbitration Timing

Bus Request BR0*
(from Master to Arbiter)
Bus Grant BG0*
(from Arbiter to Master)
Bus Grant Abort BGABT*
(from Arbiter to all Masters)

ISB Write Cycle Timing

Address A(0:19),AP (driven by Master)
Data D(0:15),DP (driven by Master)
Address Valid ADV* (driven by Master)
Read Direction RDIR (driven by Master)
Data Transfer Ack. DTACK* (driven by Slave)
Startup ROM Ena. SUROME* (driven by Master)
Bus Timeout BTMO* (driven by Master)
Address Parity Error APE* (driven by non-EFC Slave)
Data Parity Error DPE* (driven by Slave)
Corrected Data Error CDE* (not driven during writes)
Address Range Error ARE* (driven by non-EFC Slave)

ISB Read Cycle Timing

Address A(0:19),AP (driven by Master)
Data D(0:15),DP (driven by Slave)
Address Valid ADV* (driven by Master)
Read Direction RDIR (driven by Master)
Data Transfer Ack. DTACK* (driven by Slave)
Startup ROM Ena. SUROME* (driven by Master)
Bus Timeout BTMO* (driven by Master)
Address Parity Error APE* (driven by non-EFC Slave)
Data Parity Error DPE* (not driven during reads)
Corrected Data Error CDE* (driven by Slave)
Address Range Error ARE* (driven by non-EFC Slave)

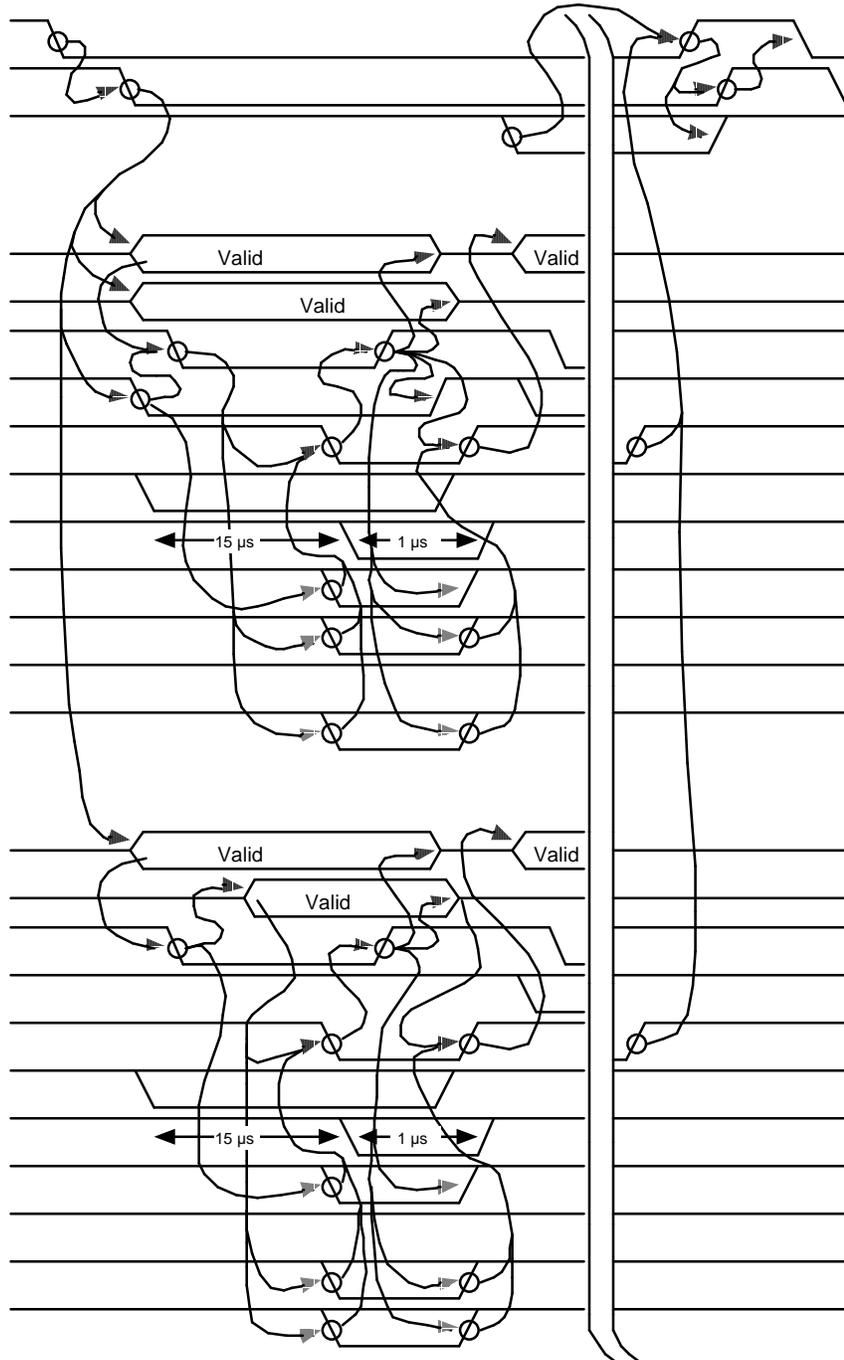


Figure 3-2 SLAVE READ TIMING

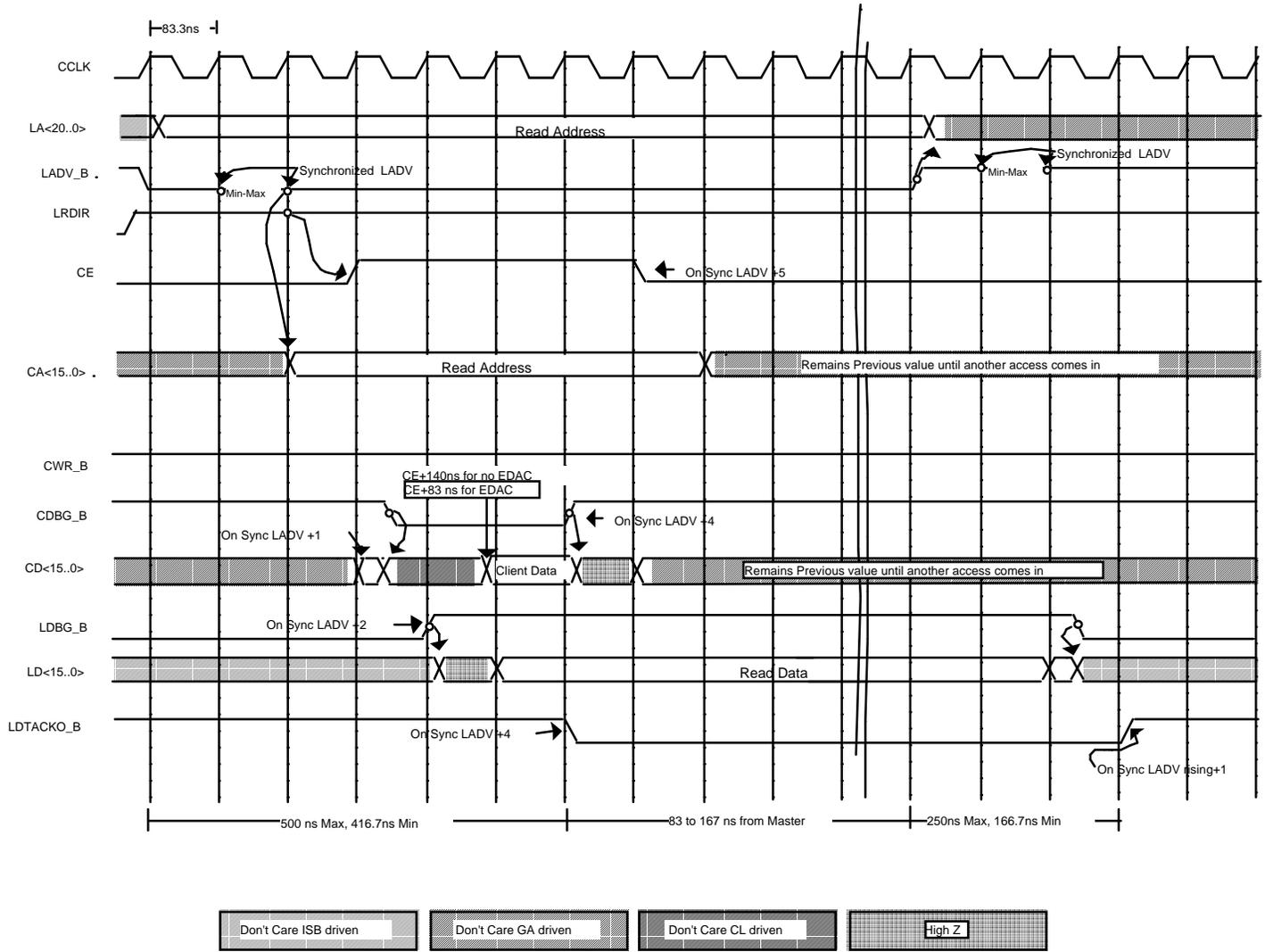
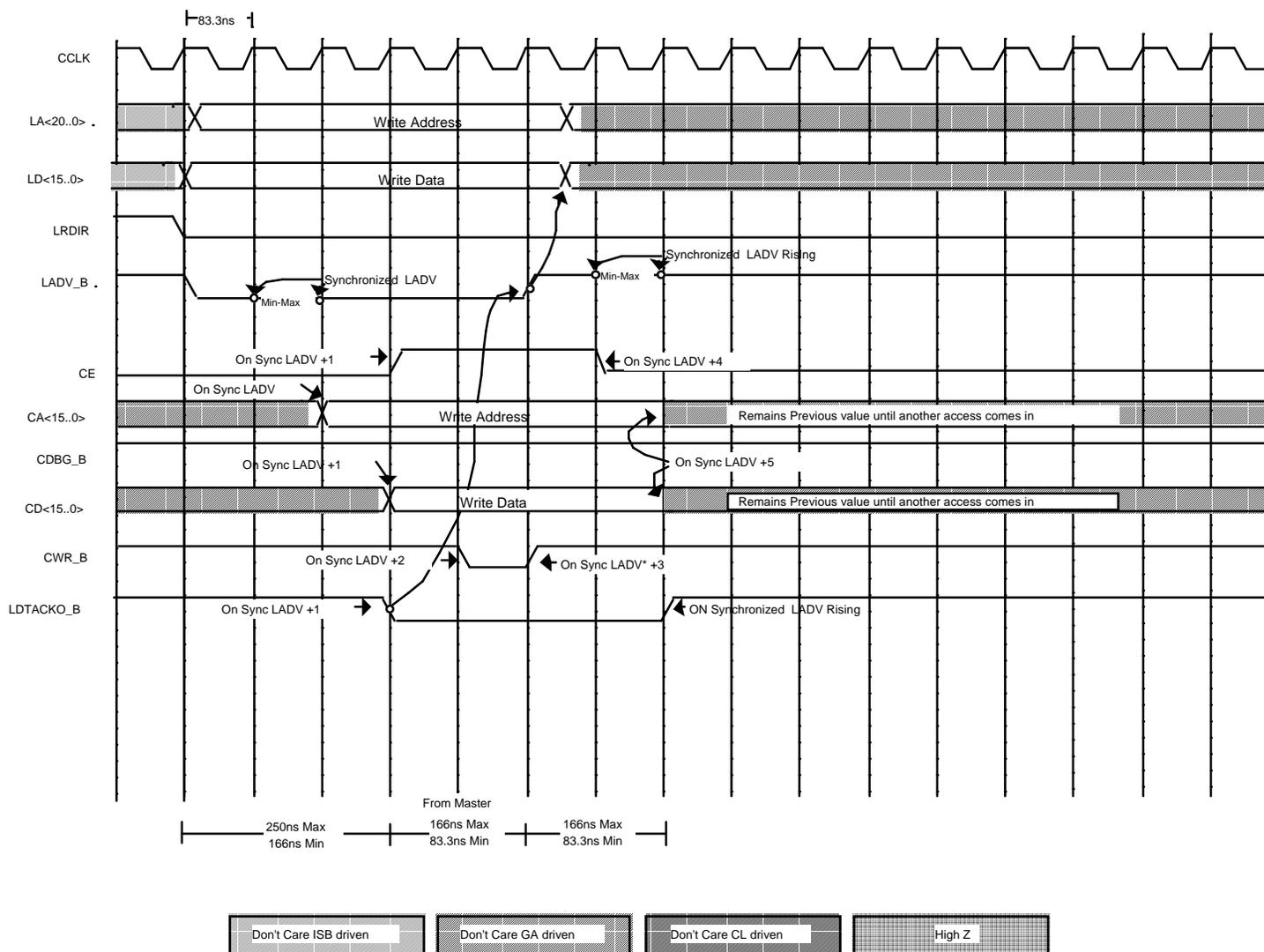


Figure 3-3 SLAVE WRITE TIMING



4. TESTABILITY CONSTRUCTS

4.1 Internal Scan

All of the latch elements used in the core area of this gate array will have scan capability. Method of scan implementation is Synopsys Test Compiler. Soft macros will have internal scan with the exception of SR flip-flops. The test compiler will not be used on soft macros. The Manchester Decoder (MANDEC) macro will have a separate scan test in which the decoder outputs "Manchester serial data clock", "Manchester serial data output", "take Manchester data", "valid Manchester word", "Manchester scan data output" and "command/data sync" will be made available externally by multiplexing.

Scan Signals: I/O pins assigned to scan test functions include the signals "scan data in", "scan data out", "scan clock", "scan mode enable", "scan clock mode enable", "Manchester test select" and "Manchester scan clock". The system clock will be used as the scan clock except for the Manchester Decoder test.

Miscellaneous Test Outputs: The SLV_XOR and BEN_XOR outputs have been added to provide observability by bringing out the exclusive-or of various nodes that are difficult to observe otherwise.

4.2 Boundary Scan

The JTAG (IEEE-1149.1 standard for boundary scan) will be implemented for this gate array. Five signals will be used for JTAG testing: "JTAG Test Data Out", "JTAG Test Data In", "JTAG Test Mode Select", "JTAG Test Clock" and "JTAG Test Reset".

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5. ELECTRICAL CHARACTERISTICS

5.1 Electrical Test Requirements

Test	Subgroups (Per MIL-STD-883, Method 5005, Table 1)
Pre Burn-In	1, 7
Post Static I Burn-In	1*, 7*
Delta Calculations *, **	
Post Static II Burn-In	1*, 7*
Delta Calculations *, **	
Post 240 Hour Burn-In	1*, 2, 3, 4***, 7*, 8, 9, 10, 11
Delta Calculations *, **	
Group B End Points ****	1, 2, 3, 4***, 7, 8, 9, 10, 11

Table 5-1 Electrical Test Requirements

- * PDA applies to these subgroups.
- ** Delta limits of Table 5-7 herein shall apply.
- *** Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after process or design changes that may affect the value.
- **** Group B.5 life test shall be performed using the dynamic burn-in configuration of Table 5-6 herein. The Table 5-7 delta limits shall apply to the life test.

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5.2 Absolute Maximum Ratings

Symbol	Parameter	Ratings		Units
		Min.	Max.	
V _{DD}	DC Supply Voltage	-0.3	7.0	V
V _{IN} , V _{OUT}	Voltage on Any Pin	- 0.3	V _{DD} + 0.3	V
I _{IN}	DC Input Current		±10	mA
P _D	Power Dissipation		TBD	mW
T _{ST}	Storage Temperature Range	-65	150	°C
T _S	Lead Temperature (Soldering, 5 seconds)		300	°C
T _J	Junction Temperature		175	°C
Θ _{JC}	Thermal Resistance, Junction to Case		1.3 **	°C/W
V _{ESD}	ESD Protection *	< 2000		V
ILU	Latchup immunity		±150 (500 ms pulse)	mA

Table 5-2 Absolute Maximum Ratings

* ESD test method conforms to MIL-STD-883, Method 3015, Electrostatic Discharge Sensitivity Test.

** This value is measured per MIL-STD-883, Method 1012.

Notes:

1. All voltages are referenced to VSS.
2. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.3 Recommended Operating Conditions

Symbol	Parameter	Ratings		Units
		Min.	Max.	
V _{DD}	Supply Voltage	4.5	5.5	V
T _C	Case Temperature	-55	125	°C
V _{IN}	Input Voltage	0	V _{DD}	V
f _{max}	Max. Operating Frequency		12.5	MHz

Table 5-3 Recommended Operating Conditions

5.3.1 Nominal Clock Specification

The ISBGA shall operate on a clock input with the following characteristics:

Frequency: 12.5 MHz to DC

Duty Cycle: 50% ± 5%

Rise Time (10% to 90%): 0.5 to 5 ns

Fall Time (10% to 90%): 0.5 to 5 ns

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5.4 DC Characteristics

5.4.1 DC Electrical Performance Characteristics

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V _{IL}	Low-level input voltage ⁵			.3 V _{DD}	V
	CMOS inputs TTL-level inputs (TCK, TDI, TMS, TRS)			0.8	V
V _{IH}	High-level input voltage ⁵		.7 V _{DD}		V
	CMOS inputs TTL-level inputs (TCK, TDI, TMS, TRS)		2.2		V
V ₋	Negative going threshold voltage Schmitt trigger inputs			1.0	V
V ₊	Positive going threshold voltage Schmitt trigger inputs		4.0		V
V _h	Typical range of hysteresis ¹ Schmitt trigger inputs		1.5	2.0	V
I _{IN}	Input leakage current				
	CMOS and Schmitt trigger inputs	V _{IN} = V _{DD} or V _{SS}	-1	1	μA
	TTL-level inputs (TCK, TRS)	V _{IN} = V _{DD} or V _{SS}	-1	1	μA
	TTL-level inputs with pull-ups (TMS, TDI)	V _{IN} = V _{DD} V _{IN} = V _{SS}	-10 -900	10 -150	μA μA
V _{OL1}	Low-level output voltage CMOS outputs ⁸	I _{OL} = 1.0 μA		0.05	V
V _{OL2}	Low-level output voltage CMOS outputs	I _{OL} = 100 μA		0.25	V
	TTL-level output (TDO)	I _{OL} = 4 mA		0.4	V
V _{OH1}	High-level output voltage CMOS outputs ⁸	I _{OH} = -1.0 μA	V _{DD} - 0.05		V
V _{OH2}	High-level output voltage CMOS outputs	I _{OH} = -100 μA	V _{DD} - 0.25		V
	TTL-level output (TDO)	I _{OH} = -4 mA	2.4		V
I _{OZ}	Three-state output leakage current				
	CMOS buffers TTL-level output (TDO)	V _O = V _{DD} or V _{SS} V _O = V _{DD} or V _{SS}	-10 -10	10 10	μA μA
I _{OS}	Short-circuit output current ^{1, 2}	V _{DD} = 5.5 V, V _O = V _{DD}	-100	100	mA
		V _{DD} = 5.5 V, V _O = 0 V	-100	100	mA
C _{IN}	Input capacitance ³				
	CMOS and TTL-level inputs Schmitt trigger inputs	F = 1 MHz @ 0 V F = 1 MHz @ 0 V		16 10	pF pF
C _{OUT}	Output capacitance ³ CMOS output buffer	F = 1 MHz @ 0 V		20	pF
C _{IO}	Bidirectional I/O capacitance ³	F = 1 MHz @ 0 V		20	pF
I _{DDQ}	Quiescent supply current ⁶	V _{DD} = 5.5V		500	μA
I _{DDQall}	Quiescent supply current (multiple vector) ⁷	V _{DD} = 5.0V		100	μA

Table 5-4 DC Performance Characteristics

See following sheet for notes

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Notes for Table 5-4:

1. Supplied as a design limit but not guaranteed or tested.
2. Not more than one output may be shorted at a time for a maximum duration of one second.
3. Capacitance measured for initial qualification or design changes which may affect the value.
4. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions:
 - a. $V_{IH} = V_{IH(min)} + 20\%$, -0% ; $V_{IL} = V_{IL(max)} + 0\%$, -50% , as specified herein, for CMOS- compatible inputs.
 - b. Devices may be tested using input voltage within the above specified range, but are guaranteed to $V_{IH(min)}$ and $V_{IL(max)}$.
5. All input and output buffers including the bi-directional buffers are identified in Table 2-1 on sheets 10 through 14
6. I_{DDQ} is measured at $V_{DD} = 5.5V$ and three temperature conditions: T_A (ambient temperature) at $-55\text{ }^\circ\text{C}$, $25\text{ }^\circ\text{C}$ and $125\text{ }^\circ\text{C}$.
7. I_{DDQall} is a quiescent supply current limit for I_{DDQall} testing as described in section 5.4.2. This limit is used as a GO/NO GO limit and is subject to change after characterization. I_{DDQall} testing will be done at $25\text{ }^\circ\text{C}$ and $V_{DD} = 5.0V$.
8. Guaranteed but not tested.

5.4.2 I_{DDQall} Testing

Refer to statement of work (SOW) Option for Flight Parts Production for I_{DDQall} testing requirements.

5.4.3 Pull-up and Pull-down Resistors

There are no pull-up or pull-down resistors used on the ISBGA except for JTAG control inputs TDI and TMS.
Note: I/O pins dedicated to scan function and JTAG for the gate array will be tied off during flight.

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5.5 AC Characteristics

5.5.1 AC Electrical Performance Characteristics

Input Pin	Output Pin	Output Transition	Test Step	Output Pin Minimum Delay	Output Pin Maximum Delay	Units
CLOCK	LDTACKE_B	HL	43	109.5	147.7	ns
CLOCK	LDBG_B	HL	45	109.6	149.1	ns
CLOCK	LDTACKO_B	HL	49	109.1	145.0	ns
CLOCK	LRDIR	ZL	1715	109.5	150.3	ns
CLOCK	LDP	ZH	1717	108.0	144.6	ns
CLOCK	LADV_B	HL	1719	108.2	141.9	ns
CLOCK	READY	LH	7965	108.7	150.3	ns
ALE	READY	HL	7941	5.3	27.5	ns
CLOCK	BCGRANT	LH	7951	107.9	145.7	ns
CLOCK	CDBG_B	HL	7956	109.0	146.8	ns
CLOCK	BCAD<0>	ZL	7965	108.9	146.3	ns
CLOCK	BCDO	LH	7965	109.2	153.9	ns
CLOCK	CD<0>	ZL	7981	108.7	145.8	ns
CLOCK	CD<15>	ZL	7981	108.7	145.8	ns

Table 5-5 AC Performance Characteristics

- Note: 1. All Functional tests at 2 MHz, Scan tests at 1 MHz and "At speed" tests at 12.5 MHz minimum must pass at VDD = 4.5V, 125 °C and at VDD = 5.5V, -55 °C.
 2. For AC tests using the CLOCK input pin, the actual delay is the specification limit minus 100 ns to account for the delay in input transitions in the tester cycle.

For the ISBGA, use the following general guidelines (under worst case temperature, voltage, process, radiation and aging conditions):

- Maximum propagation delays either rise or fall time are not to exceed the limits specified in Table 5-5 assuming 50 pF output load.
- For sequential elements (These requirements will be verified by simulation; testing is not required):
 12.5 MHz max. chip operating frequency with 60%-40% duty cycle; max. setup time = 25 ns; min. hold time = 10 ns

5.5.2 Timing Analysis

Pre-layout and post-layout timing margins shall meet the manufacturer's requirements for timing analysis. Refer to "Additional Requirements" on sheet 5 for more details.

5.5.2.1 Pre-Layout Timing Margins

Pre-layout timing margins shall be calculated by using standard extreme-value analysis. The extreme values for the cell library will be supplied by the manufacturer. Manufacturer shall assure a pre-layout match within 0.2 ns per cell between the timing numbers generated by their Valid tool kit and those generated by their golden simulator. Pre-layout timing models supplied by the manufacturer shall also check for all possible timing violations, which shall include but not be limited to setup time, hold time, minimum pulse width violations, etc. These timing models shall be comprehensive to cover pin-to-pin skew, rise time and fall time, etc. Any restrictions such as conformance to fully synchronous scan design, limitations on number of clocks used, hardwired clock trees, limitations as they relate to use of manufacturer's ATPG software, etc., shall be written and given to JPL in advance to make any changes in time if necessary. Critical paths will be identified before layout and margins will be calculated via Valid or manufacturer software tool sets, or a combination thereof.

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5.5.2.2 Post-Layout Timing Margins

Manufacturer shall maintain the hierarchy of a design as much as possible to minimize various skews when it comes to placement. Post-layout analysis of the device shall show positive margin on all identified critical paths over all operating conditions. The analysis follows the same form as the pre-layout analysis, with the post-layout timing values annotated to the design file by the manufacturer. The back annotation file shall be in Valid RapidSim compatible format. The post-layout timing parameters shall not exceed 10 % over the pre-layout values on critical paths. Timing parameters listed in section 5.5 under AC characteristics are derived from post-layout data using actual wire lengths.

5.5.2.3 Tester Specification Limits

Tester Specification limits in Table 5-5 have been adjusted for modified output levels and for differences in output loading in the Manufacturer's tester environment. Modified output levels are required to account for impedance mismatches between device outputs and the Trillium tester environment. Refer to Figure 5-3 for switching test circuits and wave forms.

5.5.3 Switching Test Circuit and Wave Forms

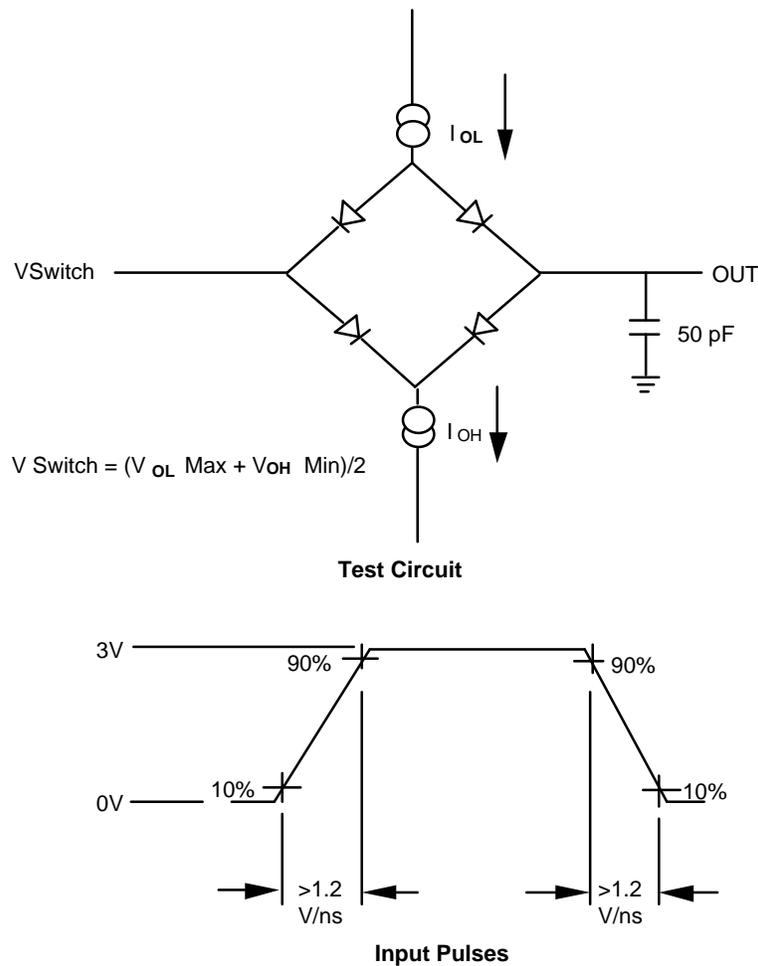


Figure 5-1 SWITCHING TEST CIRCUIT AND WAVE FORMS

1/ This capacitance is actually partially distributed through the fixturing so that the device is actually loaded by a transmission line.

Note: This is provided as an example only. A different or modified diagram may be used by the manufacturer with JPL's approval.

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SHEET 41		MICROCIRCUIT, MONOLITHIC CMOS, GATE ARRAY, INTER-SUBASSEMBLY BUS ASIC	SHEET 41

5.6 Burn-In

5.6.1 Static Burn-In

The Static Burn-In conditions per MIL-STD-883 Method 1015 shall be as specified in JPL General Specification CS 515577, Rev. C. The burn-in configurations shall be as shown in Table 5-6.

5.6.2 Dynamic Burn-In

The Dynamic Burn-In conditions shall be as specified in JPL General Specification CS 515577, Rev. C. The burn-in configuration shall be as shown in Table 5-6.

5.6.3 Burn-In Configuration

Signal Name	Pin No.	Type ¹	Burn-In Test Connection ^{2, 3}			Description
			Static I	Static II	Dynamic ⁴	
LA<20...0>	63...73, 76...85 (See Table 2-2)	I/O	GND	VDD	VDD	ISB Address
LAP	62	I/O	GND	VDD	VDD	ISB Address Parity Bit
LD<15...0>	32...47 (See Table 2-2)	I/O	GND	VDD	VDD	ISB Data
LDP	31	I/O	GND	VDD	VDD	ISB Data Parity Bit
LDPEI_B	52	Input	GND	VDD	A9	ISB Data Parity Error In
LAPEI_B	53	Input	GND	VDD	A10	ISB Address Parity Error In
LAREI_B	54	Input	GND	VDD	A11	ISB Address Range Error In
LBTMOO_B	55	Output	GND	VDD	VDD	ISB Bus Time-out Out
LADV_B	56	I/O	GND	VDD	VDD	ISB Address Valid
LRDIR	57	I/O	GND	VDD	VDD	ISB Read Direction
LDTACKI_B	58	Input	GND	VDD	A12	ISB Data Acknowledge In
LDPEO_B	59	Output	GND	VDD	VDD	ISB Data Parity Error Out
LAPEO_B	60	Output	GND	VDD	VDD	ISB Address Parity Error Out
LAREO_B	61	Output	GND	VDD	VDD	ISB Address Range Error Out
LCDEO_B	86	Output	GND	VDD	VDD	ISB Corrected Data Error Out
LBTMOI_B	92	Input	GND	VDD	A13	ISB Bus Time-out In
LDTACKO_B	93	Output	GND	VDD	VDD	ISB Data Acknowledge Out
LDTACKE_B	94	Output	GND	VDD	VDD	Local Data Acknowledge Enable
LSUROMEI_B	95	Input	GND	VDD	A14	ISB Startup ROM Enable
LDBG_B	96	Output	GND	VDD	VDD	Local Data Bus Enable
LRESET_B	87	Input	GND	VDD	V12	Warm Boot: Synchronous Reset to ISBGA
CLOCK	17	Input	GND	VDD	1.0 MHz	Global 12 MHz Gate Array Clock
BCAD<7...0>	125...132 (See Table 2-2)	I/O	GND	VDD	VDD	BCIOU Address Lower Byte and Bidirectional Data.
BCA<15...8>	107...114 (See Table 2-2)	Input	GND	VDD	A10...A3	BCIOU Address Upper Byte.
RD_B	105	Input	GND	VDD	A12	BCIOU Read Enable
WR_B	104	Input	GND	VDD	A13	BCIOU Write Enable
ALE	103	Input	GND	VDD	A11	BCIOU Address Latch Enable
READY	102	Output	GND	VDD	VDD	BCIOU Ready Line

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BCDO	101	Output	GND	VDD	VDD	BCIOU Data Direction
UCLAMP	90	Input	GND	VDD	A14	IOU Gate Array UCLAMP Signal

Table 5-6 Burn-In Connections

Signal Name	Pin No.	Type ¹	Burn-In Test Connection ^{2, 3}			Description
			Static I	Static II	Dynamic ⁴	
BCCLK	122	Input	GND	VDD	A1	BCIOU 2 MHz processor clock
BCISOA/DSCLK	133	Output	GND	VDD	VDD	BCIOU Isolation from AACS Bus A/ Manchester Serial Data Clock
BCISOB/SDO	134	Output	GND	VDD	VDD	BCIOU Isolation from AACS Bus B/ Manchester Serial Data Out
BCINT/SDOUT	135	Output	GND	VDD	VDD	BCIOU Maskable Interrupt/Manchester Scan Data Out
BCGRANT	106	Output	GND	VDD	VDD	BCIOU Bus Grant
IOUGACLK	116	Output	GND	VDD	VDD	System Clock
CA<15...0>	187...194, 3...10 (See Table 2-2)	Output	GND	VDD	VDD	Client Address Bus
CD<15...0>	163...170, 173...180 (See Table 2-2)	I/O	GND	VDD	VDD	Client Data Bus
CECH<5...0>	140...145 (See Table 2-2)	I/O	GND	VDD	VDD	Client Error Correction Bits
CACCESS/TAKDAT	186	Output	GND	VDD	VDD	Client Access/Take Manchester Data
CE	185	Output	GND	VDD	VDD	Client Enable
CWR_B	184	Output	GND	VDD	VDD	Client Write Strobe
CDBG_B	183	Output	GND	VDD	VDD	Client Data Bus Enable
CARE	182	Input	GND	VDD	A6	Client Address Range Error
CHOLD_B	181	Input	GND	VDD	A7	Client Hold
CCLOCK	150	Output	GND	VDD	VDD	Client Clock
EFCINT_B	30	Output	GND	VDD	VDD	EFC Interrupt
COLDBOOT_B	152	Input	GND	VDD	V13	Cold Boot
EDAC	153	Input	GND	VDD	A8	Error Detection and Correction Enable
LBR<0>	11	Input	GND	VDD	A9	Local Bus Request 0
LBR<1>	13	Input	GND	VDD	A7	Local Bus Request 1
LBR<2>	19	Input	GND	VDD	A5	Local Bus Request 2
LBR<3>	21	Input	GND	VDD	A3	Local Bus Request 3
LPRIORITY	28	Input	GND	VDD	A10	Local Priority
SECONNECT	23	Input	GND	VDD	A11	Support Equipment Connected
LBG<0>	12	Output	GND	VDD	VDD	Local Bus Grant 0
LBG<1>	14	Output	GND	VDD	VDD	Local Bus Grant 1
LBG<2>	20	Output	GND	VDD	VDD	Local Bus Grant 2
LBG<3>	22	Output	GND	VDD	VDD	Local Bus Grant 3
LBGABT_B	29	Output	GND	VDD	VDD	Local Bus Grant Abort
ADDR_B	27	Output	GND	VDD	VDD	Address Direction
ADEN	26	Output	GND	VDD	VDD	Address Enable
PADDR_B	16	Output	GND	VDD	VDD	Pixel Address Direction
PADEN	15	Output	GND	VDD	VDD	Pixel Address Enable

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PSDIA	154	Input	GND	VDD	A3	Pixel Serial Data In Bus A
PSDIB	155	Input	GND	VDD	A4	Pixel Serial Data In Bus B
PIUBR	156	Output	GND	VDD	VDD	PIU Bus Request
PIUBG	157	Input	GND	VDD	A5	PIU Bus Grant
PIUINT_B/VALWD	158	Output	GND	VDD	VDD	PIU Interrupt to EFC/Valid Manchester Word

Table 5-6 Burn-In Connections (cont.)

Signal Name	Pin No.	Type ¹	Burn-In Test Connection ^{2, 3}			Description
			Static I	Static II	Dynamic ⁴	
SLAVESEL	159	Input	GND	VDD	A4	Slave Access
REGSEL	160	Input	GND	VDD	A6	Register Select
PIUREGSEL	161	Input	GND	VDD	A8	PIU Register Select
PROM	162	Input	GND	VDD	A12	PROM Enable
SLV_XOR/CDB	91	Output	GND	VDD	VDD	Test Output/Command Data Sync.
BEN_XOR	151	Output	GND	VDD	VDD	Test Output
MANTSTSEL	89	Input	GND	VDD	A16	Manchester Test Select
SCNCLK	88	Input	GND	VDD	CT	Manchester Scan Clock
TEST_SE	137	Input	GND	VDD	A17	Manchester Scan Test Enable
TEST_SI	138	Input	GND	VDD	A2	Scan Test Serial Data In
TEST_EN	136	Input	GND	VDD	A17	Scan Test Enable
TEST_SO	139	Output	GND	VDD	VDD	Scan Test Serial Data Out
TCK	121	Input	GND	VDD	A0	JTAG TAP Controller Clock
TMS	120	Input	GND	VDD	A15	JTAG TAP Controller Mode Select
TDI	119	Input	GND	VDD	A2	JTAG TAP Serial Input Data
TDO	118	Output	GND	VDD	VDD	JTAG TAP Serial Output Data
TRS	117	Input	GND	VDD	V14	JTAG TAP Reset
VDD	1, 48, 99, 146	VDD	VDD	VDD	VDD	VDD Power Pads
VSS	2, 49, 100, 147	GND	GND	GND	GND	VSS Ground Pads
VDDQ	24, 50, 75, 97, 124, 148, 171, 195	VDD	VDD	VDD	VDD	VDD Power Pads
VSSQ	25, 51, 74, 98, 123, 149, 172, 196	GND	GND	GND	GND	VSS Ground Pads

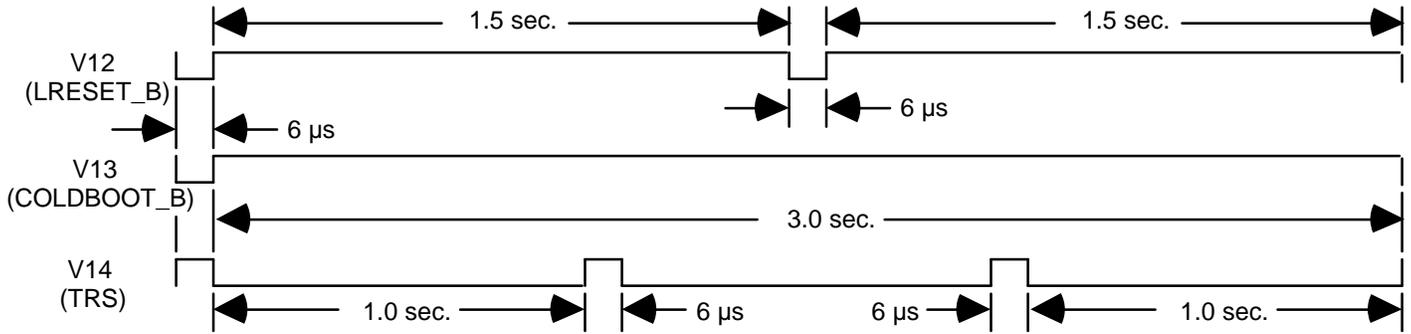
Table 5-6 Burn-In Connections (cont.)

Notes for Table 5-6:

1. I/O = Input/Output (bi-directional). Refer to sheet 14 for details on types of input buffers and output or bi-directional drivers used.
2. Unless otherwise specified, condition shall be $6.0 \text{ V} \leq V_{DD} \leq 6.5 \text{ V}$, $-0.5 \text{ V} \leq GND \leq 0.5 \text{ V}$, $V_{IL} \leq 0.8 \text{ V}$, $V_{IH} \geq 2.2 \text{ V}$ for burn-in. $V_{DD} = 6.0 \text{ V}$ nominal for life test only.
3. All inputs and outputs are connected through a $2.49 \text{ kohm} \pm 5\%$, $1/4\text{W}$ resistor. Power and Ground pins are directly connected to power and ground or some of the pins may be connected through a $2.49 \text{ kohm} \pm 5\%$ resistor to power and ground.

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SHEET 44			SHEET 44		

4. For dynamic burn-in, the master clock (CT) frequency shall be 1.0 MHz. Signals A0 through A17 shall be provided by divide by 2 counters from CT, so that $A_0 = CT/2$ or 500 kHz, $A_1 = A_0/2$ or 250 kHz, ... $A_n = A_{(n-1)}/2$, ... $A_{17} = A_{16}/2$ or approx. 3.815 Hz. Signals V12, V13 and V14 shall be generated from a vector pattern file with a clock prescale value of 6 and a variable pattern clock to generate the wave forms shown below:



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ST12187	REV. B	TITLE:	ST12187 REV. B
SHEET 45		MICROCIRCUIT, MONOLITHIC CMOS, GATE ARRAY, INTER-SUBASSEMBLY BUS ASIC	SHEET 45

5.6.4 Delta Limits

Symbol	Parameter	Spec. Limits		Units	Delta Limits	Units
		Min	Max			
I_{IL}, I_{IH}	Input Leakage Current **	-1	1	μA	± 600	nA
I_{OZL}, I_{OZH}	Three-state output leakage current CMOS buffers	-10	10	μA	± 1	μA
V_{OL2}	Low-level output voltage CMOS outputs ¹ $I_{OL} = 100 \mu\text{A}$	-	0.25	V	± 40	mV
V_{OH2}	High-level output voltage CMOS outputs ¹ $I_{OH} = -100 \mu\text{A}$	$V_{DD} - .25$	-	V	± 40	mV
I_{DDQ}	Quiescent current	-	500	μA	± 35	μA

Table 5-7 Delta Limits

1. Refer to Table 2-1 on sheets 10 through 14 for description of various input, output and bi-directional drivers/buffers used for this gate array.

** Subject to change after device characterization.

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SHEET 46			SHEET 46		

6.2 Bonding diagram

196-LEAD FLATPACK
0.470 SQ. CAVITY

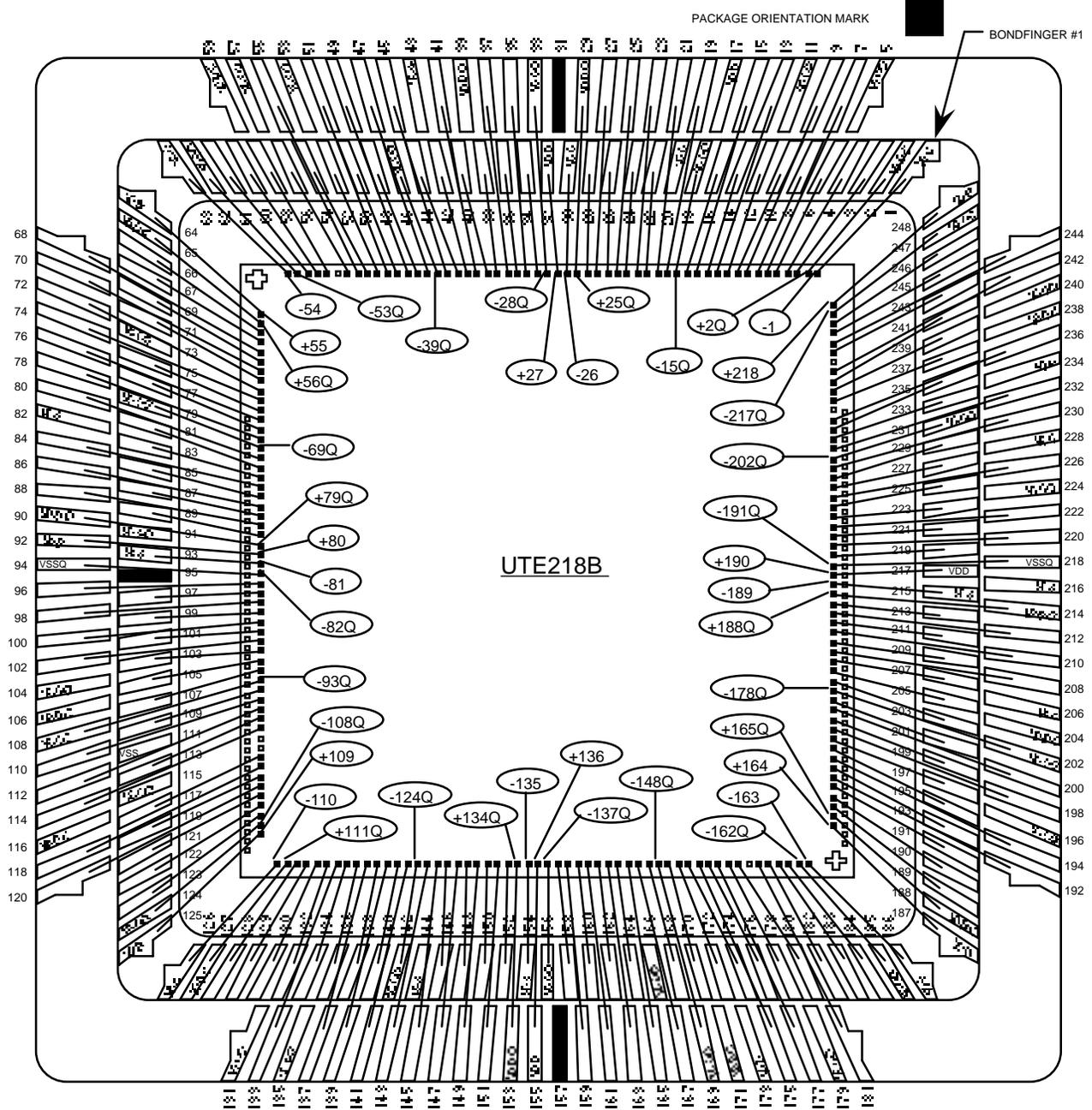


Figure 6-2 BONDING DIAGRAM (196-pin Flat Pack)

JET PROPULSION LABORATORY		CALIFORNIA INSTITUTE OF TECHNOLOGY	
ST12187	REV. B	TITLE:	ST12187 REV. B
SHEET 48		MICROCIRCUIT, MONOLITHIC CMOS, GATE ARRAY, INTER-SUBASSEMBLY BUS ASIC	SHEET 48

Table 6-1 Connections Table

Die Pad No.	Bond Finger	Package Pin No.	Die Pad No.	Bond Finger	Package Pin No.	Die Pad No.	Bond Finger	Package Pin No.	Die Pad No.	Bond Finger	Package Pin No.	Die Pad No.	Bond Finger	Package Pin No.
1	1	VSS	44	51	40	88	101	80	132	151	120	177	201	161
2	2	VDDQ	45	52	41	89	102	81	133	152	121	178	202	VSSQ
3	3	3	---	53	VSSQ	90	103	82	134	153	VDDQ	179	203	162
4	4	4	46	54	42	---	104	VSSQ	135	154	VSS	---	204	VDDQ
---	5	VSSQ	47	55	43	91	105	83	136	155	VDD	180	205	163
5	6	5	48	56	44	---	106	VDDQ	137	156	VSSQ	---	206	VSS
6	7	6	---	57	VSSQ	92	107	84	---	157	VSS	181	207	164
7	8	7	50	58	45	93	108	VSSQ	138	158	122	182	208	165
8	9	8	---	59	VDDQ	94	109	85	139	159	125	183	209	166
9	10	9	51	60	46	95	110	86	140	160	126	184	210	167
---	11	VSSQ	52	61	47	---	111	VSS	141	161	127	185	211	168
10	12	10	53	62	VSSQ	96	112	87	142	162	128	186	212	169
11	13	11	54	63	VSS	97	113	88	143	163	129	187	213	170
12	14	12	55	64	VDD	98	114	89	144	164	130	188	214	VDDQ
13	15	13	56	65	VDDQ	---	115	VSSQ	145	165	131	189	215	VSS
14	16	14	57	66	52	---	116	VDDQ	---	166	VSSQ	---	216	VSS
---	17	VDD	58	67	53	101	117	90	146	167	132	190	217	VDD
15	18	VSSQ	59	68	54	102	118	91	147	168	133	191	218	VSSQ
16	19	15	60	69	55	103	119	92	148	169	VSSQ	192	219	173
---	20	VSS	61	70	56	104	120	93	149	170	134	193	220	174
17	21	16	62	71	57	105	121	94	---	171	VDDQ	194	221	175
18	22	17	63	72	58	106	122	95	150	172	135	195	222	176
19	23	18	---	73	VSSQ	107	123	96	---	173	VDD	196	223	177
20	24	19	64	74	59	108	124	VSSQ	151	174	136	---	224	VSSQ
21	25	20	65	75	60	109	125	VDD	152	175	137	197	225	178
22	26	21	66	76	61	110	126	VSS	153	176	138	198	226	179
23	27	22	67	77	62	111	127	VDDQ	154	177	139	199	227	180
24	28	23	68	78	63	112	128	101	155	178	140	---	228	VSS
25	29	VDDQ	69	79	VSSQ	113	129	102	---	179	VSSQ	200	229	181
26	30	VSS	70	80	64	114	130	103	156	180	141	201	230	182
---	31	VSS	71	81	65	---	131	VSSQ	158	181	142	202	231	VSSQ
27	32	VDD	---	82	VSS	115	132	104	159	182	143	203	232	183
28	33	VSSQ	72	83	66	116	133	105	160	183	144	204	233	184
29	34	26	73	84	67	117	134	106	161	184	145	---	234	VSS
30	35	27	74	85	68	---	135	VSSQ	162	185	VSSQ	205	235	185
31	36	28	75	86	69	118	136	107	163	186	VSS	206	236	186
32	37	29	76	87	70	119	137	108	164	187	VDD	208	237	187
33	38	30	77	88	71	120	138	109	165	188	VDDQ	---	238	VDDQ
---	39	VDDQ	78	89	72	121	139	110	166	189	150	209	239	188
34	40	31	79	90	VDDQ	122	140	111	167	190	151	---	240	VSSQ
35	41	32	---	91	VSSQ	123	141	112	168	191	152	210	241	189
36	42	33	80	92	VDD	124	142	VSSQ	169	192	153	211	242	190
---	43	VSS	81	93	VSS	125	143	113	170	193	154	213	243	191
37	44	34	82	94	VSSQ	---	144	VSS	171	194	155	214	244	192
38	45	35	---	95	VDDQ	126	145	114	172	195	156	215	245	193
39	46	VSSQ	83	96	73	127	146	115	---	196	VSSQ	216	246	194
40	47	36	84	97	76	128	147	116	173	197	157	217	247	VSSQ
41	48	37	85	98	77	129	148	117	174	198	158	218	248	VDD
42	49	38	86	99	78	130	149	118	175	199	159			

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SHEET 49						SHEET 49	

43	50	39	87	100	79	131	150	119	176	200	160
----	----	----	----	-----	----	-----	-----	-----	-----	-----	-----

NOTE: This table establishes relationship between die pad, bond finger and package pin. All VDD bond fingers are connected to the power plane, die-attach pad and external leads 1, 48, 99 and 146. All VSS bond fingers are connected to the ground plane and external leads 2, 49, 100 and 147.

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SHEET 50			SHEET 50		

6.3 Package Outline

The design shall be compatible with package styles approved by JPL for flight parts, i.e., hermetically sealed ceramic flat packs, with strain-relieving lead bends.

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SHEET 51			SHEET 51

Figure 6-3 PACKAGE OUTLINE (196-pin Flat pack)

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ST12187	REV. B	TITLE: MICROCIRCUIT, MONOLITHIC CMOS, GATE ARRAY, INTER-SUBASSEMBLY BUS ASIC	ST12187 REV. B
SHEET 52			SHEET 52

NOTES:

1. ALL PLATED AREAS ARE GOLD PLATED OVER PLATED NICKEL UNDERCOATING PER MIL-I-38535, APPENDIX A.
2. CAPACITOR MOUNTING PADS LABELED VSS, VSSQ, VDD, OR VDDQ ARE CONNECTED TO THEIR RESPECTIVE INTERNAL POWER AND GROUND PLANES.
3. THE LID IS ELECTRICALLY CONNECTED TO VSS.
4. NUMBERING AND LETTERING ON THE CERAMIC ARE NOT SUBJECT TO VISUAL OR MARKING CRITERIA.
5. LEAD FINISH IS IN ACCORDANCE WITH MIL-I-38535, APPENDIX A.
6. APPLICATION NOTE: CAPACITOR MOUNTING PADS ARE DIMENSIONED FOR AN AVX/MIL-C-55681, P/N CDR33BX104A, 50 V, 0.1 μ F CAPACITOR.
7. DOGLEG GEOMETRIES OPTIONAL WITHIN DIMENSIONS SHOWN.
8. THESE AREAS MAY HAVE NOTCHES AND TABS DIFFERENT THAN SHOWN.
9. LEAD TRUE POSITION TOLERANCES AND COPLANARITY ARE NOT MEASURED.

FIXED EXTERNAL P & G LEAD CONNECTION TABLE

PWR, GND LEAD FUNCTION	LEAD						
VDD	1	VSS	2	VDDQ	24	VSSQ	25
VDD	48	VSS	49	VDDQ	50	VSSQ	51
VDD	99	VSS	100	VDDQ	75	VSSQ	74
VDD	146	VSS	147	VDDQ	97	VSSQ	98
				VDDQ	124	VSSQ	123
				VDDQ	148	VSSQ	149
				VDDQ	171	VSSQ	172
				VDDQ	195	VSSQ	196

Figure 6-3 PACKAGE OUTLINE (continued)

JET PROPULSION LABORATORY		CALIFORNIA INSTITUTE OF TECHNOLOGY			
ST12187	REV. B	TITLE: MICROCIRCUIT, MONOLITHIC CMOS, GATE ARRAY, INTER-SUBASSEMBLY BUS ASIC			ST12187 REV. B
SHEET 53					SHEET 53

6.4 Marking Diagram

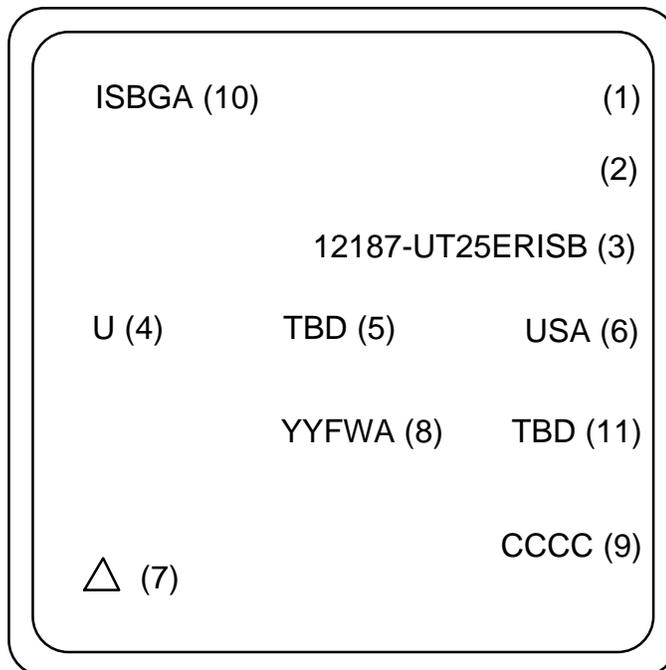


Figure 6-4 MARKING DIAGRAM

- (1) Manufacturer Part Number
- (2) QPL or QML Number, if applicable (for flight unit only)
- (3) JPL Part Number
- (4) Manufacturer Trademark
- (5) Federal Supplier Manufacturing Number
- (6) Country of Origin
- (7) Pin 1 indicator and ESD identifier
- (8) Lot Identification (Date) Code - Year and Fiscal Week of Lid Seal. YY = Year, FW = Fiscal Week, and A = Identifier for lots sealed within same week. (The first assembly lot of devices sealed does not have a designator. "A" designates the second assembly lot of devices sealed within FWXX; "B" designates the third assembly lot of devices sealed within FWXX, etc. Letters "I", "O" and "Q" shall not be used.) "Q" suffix for life test parts, if applicable, shall be added to the Date Code.
- (9) Serialization (Traceability Capability to Die)
- (10) Chip Name
- (11) Manufacturer Lot Number (optional, format to be determined by Manufacturer)

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SHEET 54			SHEET 54

7. DEVICE STATISTICS

- Total Port signals
 - Inputs 38
 - Outputs 50
 - Bidirectional 71
- Testability signals
 - Scan Test Inputs 5
 - Scan Test Output 1
 - JTAG TAP Inputs 4
 - JTAG TAP Output 1
- Total VSS and VDD 24 pins
- Unused (not connected) 2 pins
- Cell and block counts:
 - Cells 5,696
 - Blocks 73
- p and n-transistor counts:
 - p: 55,379 n: 55,379
- Number of gates: 23,074 gates
- Functional patterns @ 2 MHz and Scan patterns @ 1 MHz are used to achieve 98.5% Port fault coverage at cell boundaries. Separate patterns are used for ac delay measurements and “at-speed” tests @ 12.5 MHz.
- As indicated in section 4.1, the ISB gate array will have full internal scan implementation and JTAG 1149.1 boundary scan when it is released to the manufacturer.

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SHEET 55			SHEET 55

8. EXCEPTIONS TO CS515577C:

The following are the applicable exceptions to JPL Specification CS515577, Rev. C:

- Page 3, Para. 2.1 Change “MIL-M-38510H, Microcircuits, General Specification for, including amendments 1 through 5” to “MIL-I-38535, Integrated Circuits (Microcircuits) Manufacturing, General Specification for”
- Change “MIL-STD-883C, Test Methods and Procedures for Microelectronics, including Notices 1-12, except substitute for Method 1019 the text of ‘MIL-STD-883, Proposed Method 1019.4’ dated 1/28/91” to “MIL-STD-883, Test Methods and Procedures for Microelectronics”
- Pages 3 through 11 All references to MIL-M-38510 paragraphs shall be deemed to refer to the corresponding paragraph of Appendix A to MIL-I-38535.
- Page 6, Para. 3.8 a Change “Lot traveler(s)” to “Documentation”
- Page 6, Para. 3.8 b Change to read “Electrical test program, for review but not for approval.”
- Page 6, Para. 3.10 a Change to read “Any interim or post-burn-in room temperature test failures.”
- Page 8, Para. 4.3.6 Change “Three (3) control units” to “One (1) control unit”
- Change “control units” to “control unit” throughout the paragraph.
- Add at end of paragraph: “The manufacturer may replace the use of control units with an alternative procedure based on statistical process controls (SPC) for verification and calibration of automatic test equipment, including load boards. The alternative procedure shall be submitted to JPL for review and approval prior to testing flight parts.”
- Page 8, Para. 4.5.6 Delete “except that the MIL-STD-883 Method for total dose (subgroup 2) shall be Method 1019.4 (proposed revision dated 1/28/91) except that the dose rate (paragraph 3.5) shall be 100 rad(Si)/s.”
- Page 8, Para. 4.5.6.2 Delete “(substituting the 1/28/91 draft of Method 1019.4)”
- Page 8, Para. 4.5.6.2.1 Delete this paragraph and substitute “Time dependent effects (TDE) testing is not required for this device.”
- Page 8, Para. 4.6.5 Add new paragraph as follows: “The manufacturer may substitute an alternative procedure for 100% non-destructive bond pull (NDBP). The procedure shall include provisions for visual inspection of bonding pads and posts, and statistical process controls (SPC) for automatic bonding equipment. The alternative procedure shall be submitted to JPL for review and approval prior to assembly of flight parts.”
- Page 8, Para. 4.8.1 a Change to read “A copy of summary documentation for screening and QCI. Completed screening and QCI lot travelers shall be made available for review by JPL at the manufacturer’s facility, but are not required to be shipped as part of the data package.”

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